Table 7-7. A1 Troubleshooting

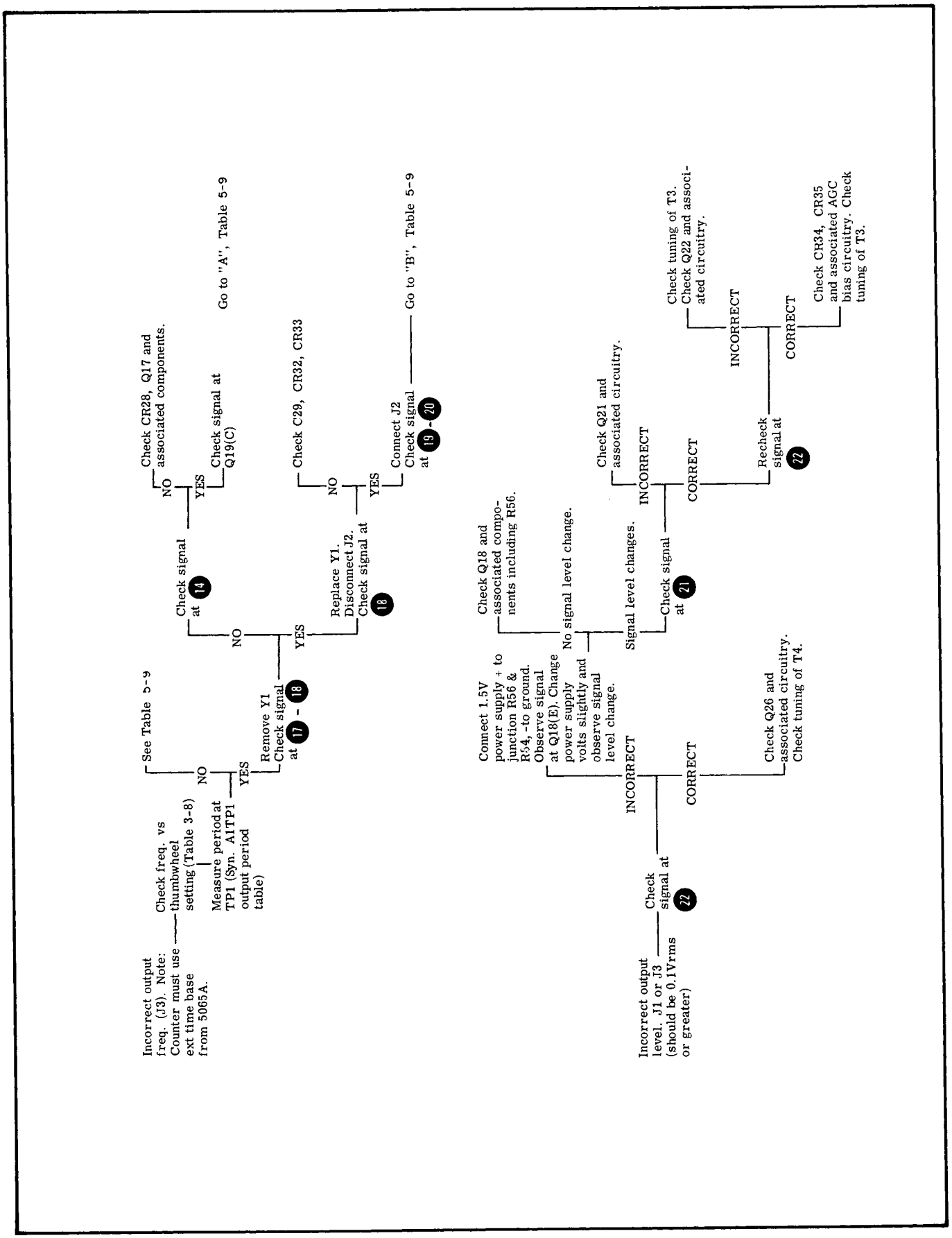
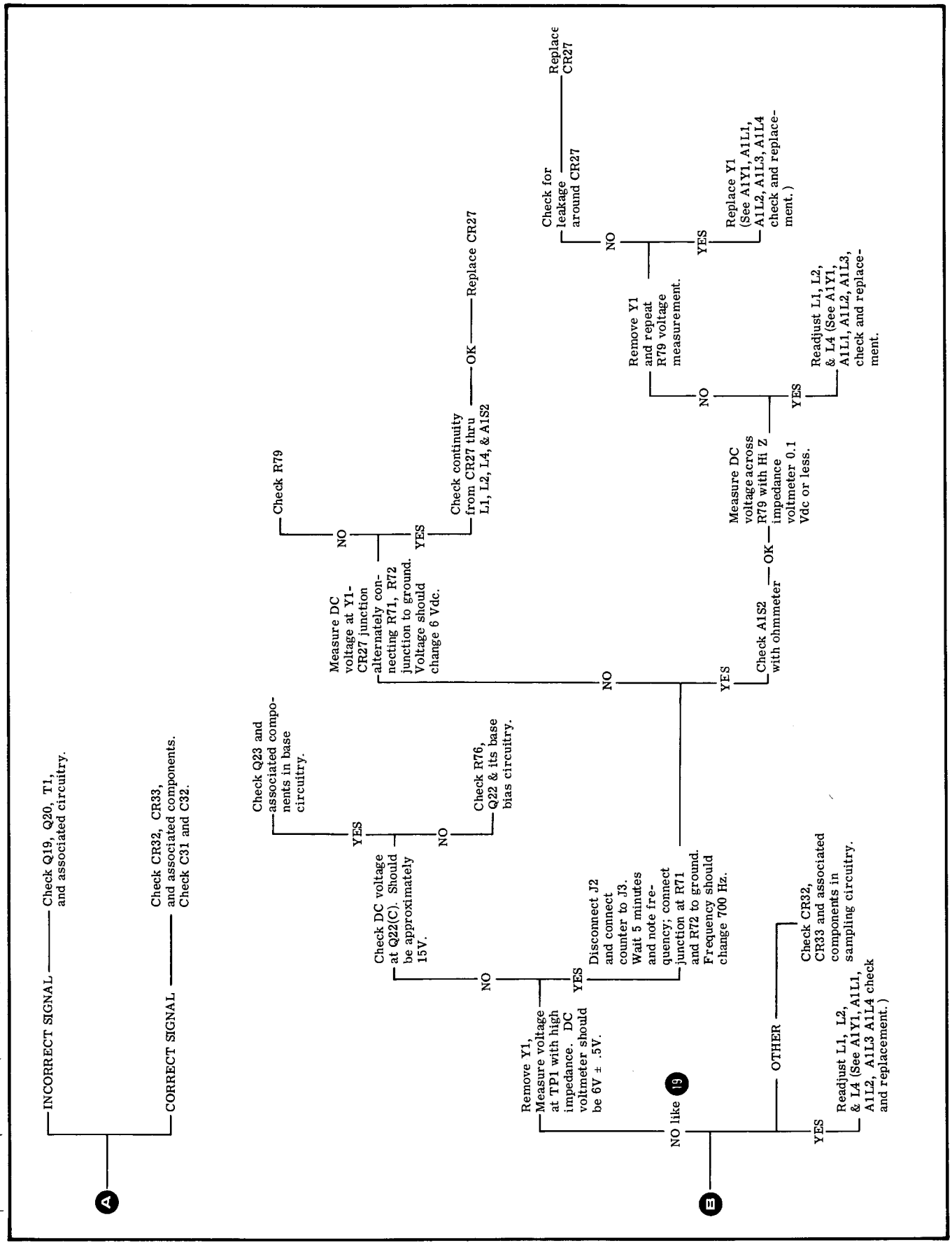


Table 7-8. A1 Troubleshooting



AC AMPLIFIER A7 THEORY

The Ac Amplifier is a low noise, high gain amplifier. This amplifier receives a low-level signal from A12 RVFR Assembly and provides an ac output proportional to amplitude and phase of the fundamental frequency of the input signal. At resonance, the input contains a large amount of 274 Hz second harmonic and a small amount of 137 Hz fundamental. The amplified 137 Hz fundamental is separated from the second harmonic, amplified, and applied to A8 Phase Detector Assembly. The 137 Hz output is also routed to A14 Logic Assembly as one logic input. The 274 Hz second harmonic is amplified, rectified, and routed to A14 Assembly as another logic input. These logic inputs are two of the signals which control the CONTINUOUS OPERATION lamp on the front panel. The Ac Amplifier also furnishes PHOTO I and 2ND HARMONIC inputs to the CIRCUIT CHECK meter.

The input signal, some 137 Hz but mostly 274 Hz at resonance, couples through J1. Input stage Q1 and Q2 form a low noise differential amplifier which feeds the push-pull inputs of IC1 that provides high gain. Note that the input at IC1(2) is ac-shunted to ground by C4. Thus the ac input to IC1 is single ended while the dc input is a balanced differential input. In addition, the feedback from IC1(6) to Q1 base treats ac and dc separately. This technique results in a preamplifier circuit that constitutes a transfer impedance; i.e., input is current and output is voltage. This impedance amounts to 2×10^7 ohms for ac and 10^5 ohms for dc. Thus for a 1μ a input signal, the output voltages is $10^{-6} \times 2 \times 10^{-7} = 20$ volts. R3 adjusts the input to zero volts dc. Zeners CR1 and CR2 provide +14.7 volts for IC1. Feedback to Q1 base restricts frequency response to approximately 6 kHz.

There are three IC1 outputs: (1) the twin-T filter connecting to Q5 and Q6, (2) the 2nd harmonic adjustment R19 and, (3) TP2 and the connection through A17(6) to the PHOTO I position of the CIRCUIT CHECK meter. The twin-T filter circuit works with Q5 and Q6 to give sharp rejection to the 274 Hz component of the input signal. The filtered 137 Hz component is amplified in IC2 and routed to A8 Phase Detector Assembly. Q8 serves to impedance match the notch filter circuit to the loop gain control R32. With R32 properly set, the ac amplifier (Q8, R32, and IC2) gain is about 40 dB. Zeners Q6 and Q7 provide $\pm$9.1 volts for IC2. Dc feedback from IC2(6) to IC2(2) sets IC2 gain.

The signal at 2nd harmonic adjustment R19 (which is mostly 274 Hz at resonance) is amplified, rectified, and then dc amplified in the 2nd harmonic detector circuit for a logic output to A14 Logic Assembly. Q3 and Q7 act as forward amplifiers, with Q4 functioning as a feedback amplifier. The RC components in Q7 collector circuit provide frequency compensation. Diodes CR4 and CR5 provide a rectified dc proportional to the input. Emitter follower Q9 feeds the 2nd harmonic output to the A14 Logic Assembly.

A7 MAINTENANCE

NORMAL OPERATION

a. Preamplifier A7Q1, Q2, and IC1 act as a transfer impedance, i.e, this circuit is designed to work from a current source and deliver a voltage output proportional to the current input. The equivalent transfer impedance of this preamplifier circuit is 2×10^7 ohms for ac signals and 10^5 for dc signals.

b. The notch filter circuit is set to notch out the second harmonic content of the modulation frequency (274 Hz).

c. The ac amplifier circuit of Q8 and IC2 has a gain of 40 dB adjustable by R32.

d. The second harmonic detector circuit amplifies and detects the preamplifier output, which is mostly 274 Hz at resonance. The dc output of this circuit routes to A14 Logic Assembly and to the 2ND HARMONIC position of the CIRCUIT CHECK switch.

OPERATIONAL CHECK

NOTE

This check need only be performed if trouble is suspected in the A7 Assembly.

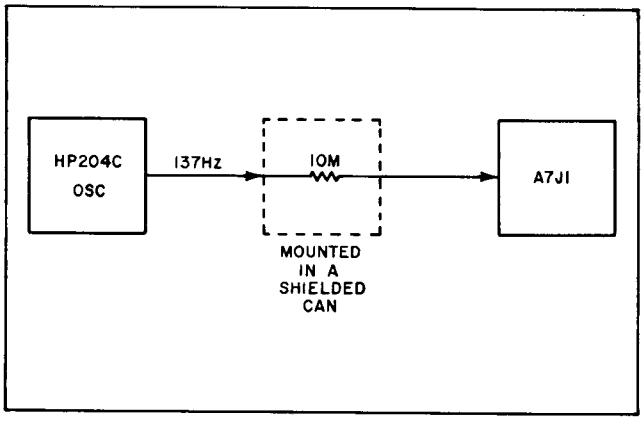
a. A quick check of the A7 Assembly can be made by monitoring the output (yellow lead) with an oscilloscope, removing the input cable from A7J1 and, using a small metal tool, touching the center conductor of A7J1. The hum signal thus induced will cause a saturated or clipped signal to appear on the oscilloscope. This maximum signal output will peg the CIRCUIT CHECK meter when switched to 2ND HARMONIC.

b. A more precise test can be made by use of the following procedure.

1) Set up equipment as shown in A7 Test Setup. Use Micon-to-BNC test cable that is supplied, for the connection to A7J1.

2) Set oscillator frequency to 137 Hz and output level to .5 V peak-to-peak.

A7 Test Setup



3) Connect oscilloscope to A7TP2. Output should be about 1V peak-to-peak.

4) Connect oscilloscope to A7TP1. Signal should be about 0.5 V peak-to-peak.

5) Connect oscilloscope to A7 output (yellow lead). Signal gain at this point with respect to the signal level at A7TP1 can be varied from zero to approximately 100 by R32. With R32 set for proper loop gain, the A7 output signal will be roughly 10 to 40 times the signal at A7TP1.

6) Set CIRCUIT CHECK meter switch to 2ND HARMONIC. Reduce oscillator output and allowing for a time lag, note the CIRCUIT CHECK meter response. Meter should follow oscillator level setting. This procedure checks the second harmonic detector circuit of the A7 Assembly.

7) Remove the test setup and oscilloscope connections. Using the Micon-to-BNC test cable provided, connect a dc voltmeter to A7J1. DC voltage at this point should not exceed ±5 mV. Excessive dc voltage at this point will result in a noisy solar cell (A12 RVFR Assembly) output. Adjust A7R3 to bring this voltage below ±5 mV if required.

8) Remove test cable and dc voltmeter. Reconnect cable from A12 Assembly to A7J1.

TROUBLESHOOTING AND REPAIR

a. If any components in the preamplifier circuit are replaced, connect a voltmeter to A7Q1 base and adjust A7R3 for less than 0.5 mV at this point.

b. After any repairs to A7 Assembly, adjust A7R32 as described in Section 5-30, LOOP GAIN ADJUSTMENT.

MODULE REPLACEMENT

If the A7 Assembly is replaced with either a repaired or new Assembly, set A7R3 as described in the preceeding section TROUBLESHOOTING AND REPAIR. Also A7R32, the loop gain adjustment, should be adjusted as described in Section 5-30, LOOP GAIN ADJUSTMENT. Perform adjustments outlined in Paragraphs 5-27 to 5-31.

Table 7-9. A7 AC Amplifier Assembly Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A7	05065-6010	1	MODULAR ASSY:AC AMPLIFIER	28480	05065-6010
A7J1	1250-0829	1	CONNECTOR:RF 50-OHM SCREW ON TYPE	98291	50-045-4610
A7	0340-0119	1	INSULATED FEED THRU:TEFLON	98291	FT-SM-023-P20
A7	05065-0032	1	COVER:SIGNAL AMPLIFIER	28480	05065-0032
A7	05065-0033	1	CHASSIS:SIGNAL AMPLIFIER	28480	05065-0033
A7	05065-2024	1	PLATE:END	28480	05065-2024
A7A1	05065-6011	1	BOARD ASSY:SIGNAL AMPLIFIER	28480	05065-6011
A7A1C1	0180-0116	1	C:FXD ELECT 6.8 UF 10% 35VDCW	56289	150D685X9035B2-DYS
A7A1C2	0180-0106	4	C:FXD ELECT 60 UF 20% 6VDCW	28480	0180-0106
A7A1C3	0160-0340	2	C:FXD MICA 600 PF 1%	28480	0160-0340
A7A1C4	0180-0291	1	C:FXD ELECT 1.0 UF 10% 35VDCW	56289	150D105X9035A2-DYS
A7A1C5	0180-0113	1	C:FXD ELECT TA 100UF +20-15% 30VDCW	56289	109D107C2030T2
A7A1C6	0160-0340		C:FXD MICA 600 PF 1%	28480	0160-0340
A7A1C7	0160-0158	1	C:FXD MY 0.0056 UF 10% 200VDCW	56289	192P56292-PTS
A7A1C8	0140-0220	1	C:FXD MICA 200 PF 1% 300VDCW	28480	0140-0220
A7A1C9	0170-0086	1	C:FXD MY 0.22UF 20% 50VDCW	84411	601PE STYLE 3
A7A1C10	0180-0197	3	C:FXD ELECT 2.2 UF 10% 20VDCW	56289	150D225X9020A2-DYS
A7A1C11	0170-0091	2	C:FXD POLY 0.01213 UF 2% 50VDCW	56289	P146504 PYP
A7A1C12	0170-0090	1	C:FXD POLY 0.0252 UF 1% 50VDCW	56289	P246505 PYP
A7A1C13	0170-0091		C:FXD POLY 0.01213 UF 2% 50VDCW	56289	P146504 PYP
A7A1C14	0180-0160	1	C:FXD ELECT 22 UF 20% 35VDCW	28480	0180-0160
A7A1C15	0150-0093	1	C:FXD CER 0.01 UF +80-20% 100VDCW	72982	801-K800011
A7A1C16	0180-0197		C:FXD ELECT 2.2 UF 10% 20VDCW	56289	150D225X9020A2-DYS
A7A1C17	0160-0168	1	C:FXD MY 0.1 UF 10% 200VDCW	56289	192P10492-PTS
A7A1C18	0180-0098	1	C:FXD ELECT 100 UF 20% 20VDCW	56289	150D107X0020S2-DYS
A7A1C19	0180-0106		C:FXD ELECT 60 UF 20% 6VDCW	28480	0180-0106
A7A1C20	0180-0197		C:FXD ELECT 2.2 UF 10% 20VDCW	56289	150D225X9020A2-DYS
A7A1C21	0180-0106		C:FXD ELECT 60 UF 20% 6VDCW	28480	0180-0106
A7A1C22	0140-0176	1	C:FXD MICA 100 PF 2%	28480	0140-0176
A7A1C23	0140-0209	1	C:FXD MICA 5.0 PF 10%	28480	0140-0209
A7A1C24	0180-0106		C:FXD ELECT 60 UF 20% 6VDCW	28480	0180-0106
A7A1CR1	1902-3203	2	DIODE BREAKDOWN:SILICON 14.7V 5%	28480	1902-3203
A7A1CR2	1902-3203		DIODE BREAKDOWN:SILICON 14.7V 5%	28480	1902-3203
A7A1CR3	1902-0025	1	DIODE,BREAKDOWN:10.0V 5% 400 MW	28480	1902-0025
A7A1CR4	1901-0025	2	DIODE:SILICON 100MA/1V	07263	FD 2387
A7A1CR5	1901-0025		DIODE:SILICON 100MA/1V	07263	FD 2387
A7A1CR6	1902-3149	2	DIODE BREAKDOWN:9.09V 5%	28480	1902-3149
A7A1CR7	1902-3149		DIODE BREAKDOWN:9.09V 5%	28480	1902-3149
A7A1IC1	1820-0058	2	IC:LIN. OP. AMP. 15K MIN.(TO-99)	07263	U5B770939X
A7A1IC2	1820-0058		IC:LIN. OP. AMP. 15K MIN.(TO-99)	07263	U5B770939X
A7A1Q1	1854-0023	5	TSTR:SI NPN(SELECTED FROM 2N2484)	28480	1854-0023
A7A1Q2	1854-0023		TSTR:SI NPN(SELECTED FROM 2N2484)	28480	1854-0023
A7A1Q3	1854-0023		TSTR:SI NPN(SELECTED FROM 2N2484)	28480	1854-0023
A7A1Q4	1854-0023		TSTR:SI NPN(SELECTED FROM 2N2484)	28480	1854-0023
A7A1Q5	1854-0003	3	TSTR:SI NPN(SELECTED FROM 2N1711)	28480	1854-0003
A7A1Q6	1854-0003		TSTR:SI NPN(SELECTED FROM 2N1711)	28480	1854-0003
A7A1Q7	1853-0001	1	TSTR:SI PNP(SELECTED FROM 2N1132)	28480	1853-0001
A7A1Q8	1854-0003		TSTR:SI NPN(SELECTED FROM 2N1711)	28480	1854-0003
A7A1Q9	1854-0023		TSTR:SI NPN(SELECTED FROM 2N2484)	28480	1854-0023
A7A1R1	0757-0965	4	R:FXD FLM 51K OHM 2% 1/8W	28480	0757-0965
A7A1R2	0698-3459	2	R:FXD MET FLM 383K OHM 1% 1/8W	28480	0698-3459
A7A1R3	2100-1659	1	R:VAR WW 5K OHM 10% TYPE P 1W	28480	2100-1659
A7A1R4	0757-0965		R:FXD FLM 51K OHM 2% 1/8W	28480	0757-0965
A7A1R5	0698-3459		R:FXD MET FLM 383K OHM 1% 1/8W	28480	0698-3459
A7A1R6	0757-0965		R:FXD FLM 51K OHM 2% 1/8W	28480	0757-0965
A7A1R7	0757-0903	1	R:FXD MET FLM 130 OHM 2% 1/4W	28480	0757-0903
A7A1R8	0757-0915	2	R:FXD FLM 430 OHM 2% 1/8W	28480	0757-0915
A7A1R9	0757-0915		R:FXD FLM 430 OHM 2% 1/8W	28480	0757-0915
A7A1R10	0757-0965		R:FXD FLM 51K OHM 2% 1/8W	28480	0757-0965
A7A1R11	0757-0928	2	R:FXD FLM 1.5K OHM 2% 1/8W	28480	0757-0928
A7A1R12	0757-0893	2	R:FXD FLM 51 OHM 2% 1/8W	28480	0757-0893
A7A1R13	0757-0931	1	R:FXD FLM 2K OHM 2% 1/8W	28480	0757-0931
A7A1R14	0757-0199	1	R:FXD MET FLM 21.5K OHM 1% 1/8W	28480	0757-0199
A7A1R15	0757-0959	1	R:FXD FLM 30K OHM 2% 1/8W	28480	0757-0959
A7A1R16	0757-0457	2	R:FXD MET FLM 47.5K OHM 1% 1/8W	28480	0757-0457
A7A1R17	0757-0976	3	R:FXD FLM 150K OHM 2% 1/8W	28480	0757-0976
A7A1R18	0757-0976		R:FXD FLM 150K OHM 2% 1/8W	28480	0757-0976
A7A1R19	2100-1761	1	R:VAR WW 10K OHM 5% TYPE V 1W	28480	2100-1761
A7A1R20	0757-0926	1	R:FXD FLM 1.2K OHM 2% 1/8W	28480	0757-0926
A7A1R21	2100-1775	1	R:VAR WW 5K OHM 5% TYPE H 1W	28480	2100-1775
A7A1R22	0757-0948	3	R:FXD FLM 10K OHM 2% 1/8W	28480	0757-0948
A7A1R23	0757-0457		R:FXD MET FLM 47.5K OHM 1% 1/8W	28480	0757-0457
A7A1R24	0757-0939	1	R:FXD FLM 4.3K OHM 2% 1/8W	28480	0757-0939
A7A1R25	0757-0924	6	R:FXD MET FLM 1K OHM 2% 1/8W	28480	0757-0924
A7A1R26	0757-0976		R:FXD FLM 150K OHM 2% 1/8W	28480	0757-0976

See introduction to this section for ordering information

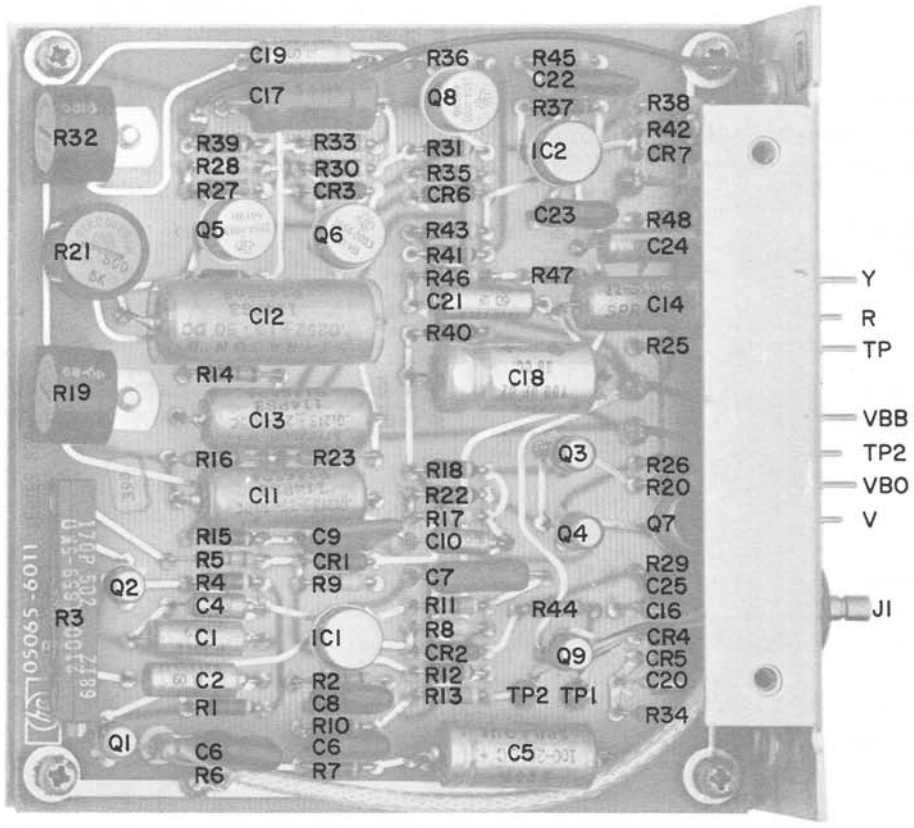
Table 7-9. A7 AC Amplifier Assembly Replaceable Parts (Continued)

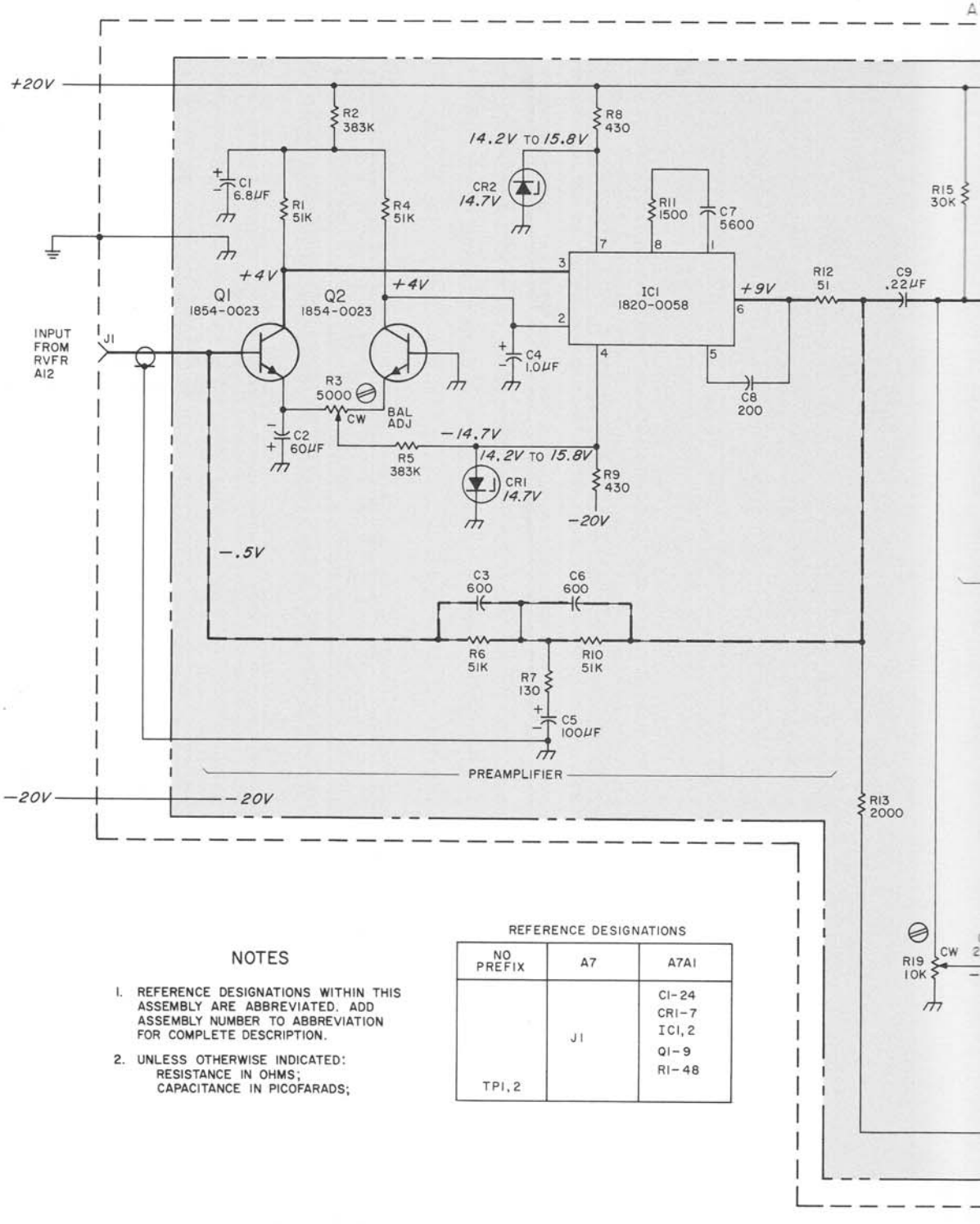
Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A7A1R27	0757-0924		R:FXD MET FLM 1K OHM 2% 1/8W	28480	0757-0924
A7A1R28	0757-0938	1	R:FXD FLM 3.9K OHM 2% 1/8W	28480	0757-0938
A7A1R29	0757-0948		R:FXD FLM 10K OHM 2% 1/8W	28480	0757-0948
A7A1R30	0757-0935	1	R:FXD FLM 3K OHM 2% 1/8W	28480	0757-0935
A7A1R31	0757-0900	2	R:FXD MET FLM 100 OHM 2% 1/8W	28480	0757-0900
A7A1R32	0757-0924		R:FXD MET FLM 1K OHM 2% 1/8W	28480	0757-0924
A7A1R33	0757-0924		R:FXD MET FLM 1K OHM 2% 1/8W	28480	0757-0924
A7A1R34	0698-3129	1	R:FXD DEPC 1.00 MEGOHM 1% 1/8W	28480	0698-3129
A7A1R36	0757-0949	1	R:FXD FLM 11K OHM 2% 1/8W	28480	0757-0949
A7A1R37	0757-0971	1	R:FXD FLM 91K OHM 2% 1/8W	28480	0757-0971
A7A1R38	0757-0921	1	R:FXD MET FLM 750 OHM 2% 1/8W	28480	0757-0921
A7A1R39	0757-0948		R:FXD FLM 10K OHM 2% 1/8W	28480	0757-0948
A7A1R40	0757-0900		R:FXD MET FLM 100 OHM 2% 1/8W	28480	0757-0900
A7A1R41	0757-0969	2	R:FXD FLM 75K OHM 2% 1/8W	28480	0757-0969
A7A1R42	0757-0924		R:FXD MET FLM 1K OHM 2% 1/8W	28480	0757-0924
A7A1R43	0757-0924		R:FXD MET FLM 1K OHM 2% 1/8W	28480	0757-0924
A7A1R44	0757-0941	2	R:FXD FLM 5.1K OHM 2% 1/8W	28480	0757-0941
A7A1R45	0757-0928		R:FXD FLM 1.5K OHM 2% 1/8W	28480	0757-0928
A7A1R46	0757-0941		R:FXD FLM 5.1K OHM 2% 1/8W	28480	0757-0941
A7A1R47	0757-0969		R:FXD FLM 75K OHM 2% 1/8W	28480	0757-0969
A7A1R48	0757-0893		R:FXD FLM 51 OHM 2% 1/8W	28480	0757-0893

Figure 7-13
A7 AC AMPLIFIER SCHEMATIC DIAGRAM

(See Page 7-35)

Figure 7-12. A7 AC Amplifier





NOTES

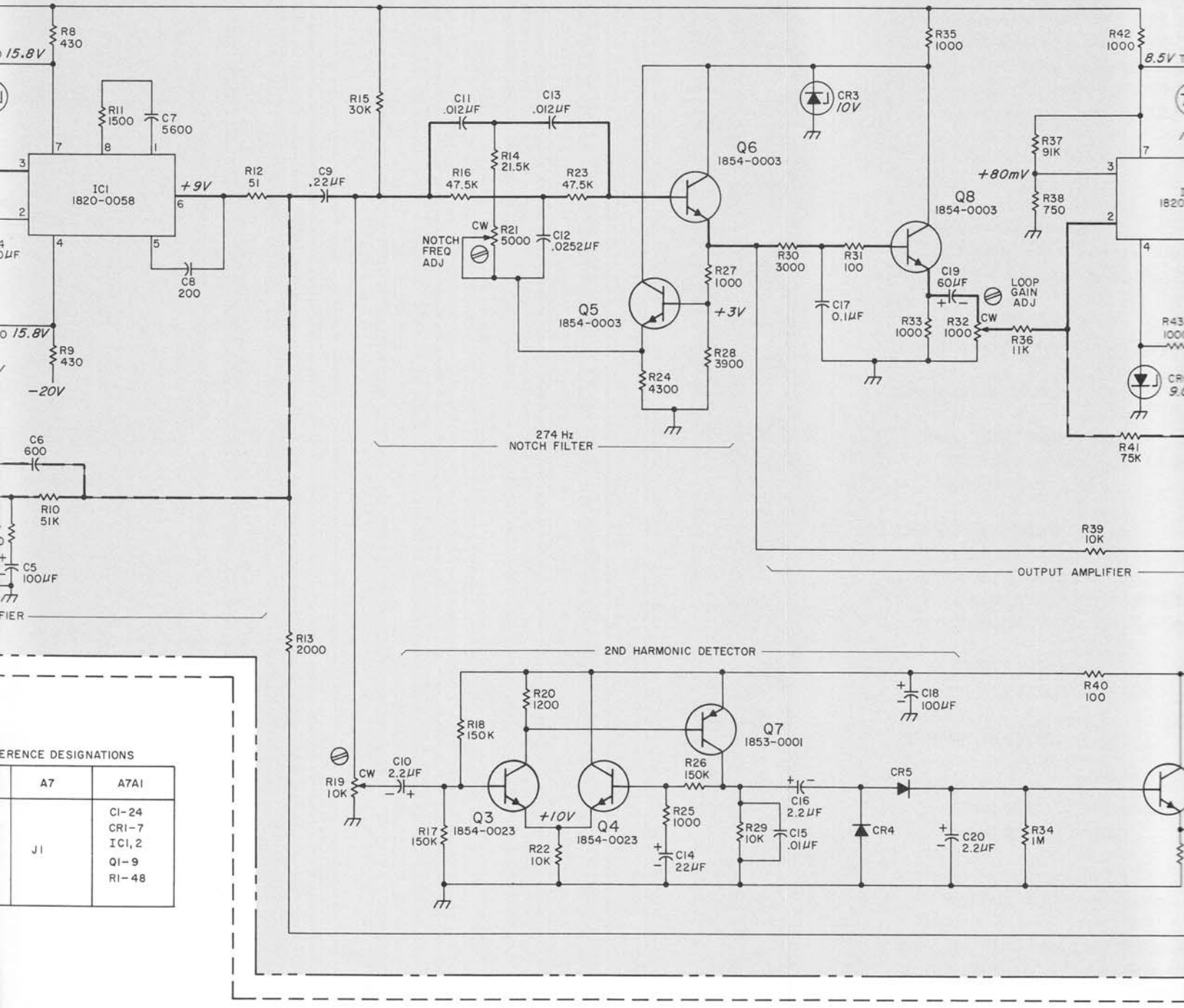
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

NO PREFIX	A7	A7A1
TP1, 2	J1	C1-24 CR1-7 IC1, 2 Q1-9 R1-48

A7 AC AMPLIFIER ASSEMBLY (05065-6010) (NOTE 1)

A7A1 AC AMPLIFIER BOARD (05065-6011)



ERENCE DESIGNATIONS

	A7	A7A1
	J1	C1-24 CR1-7 IC1, 2 Q1-9 R1-48

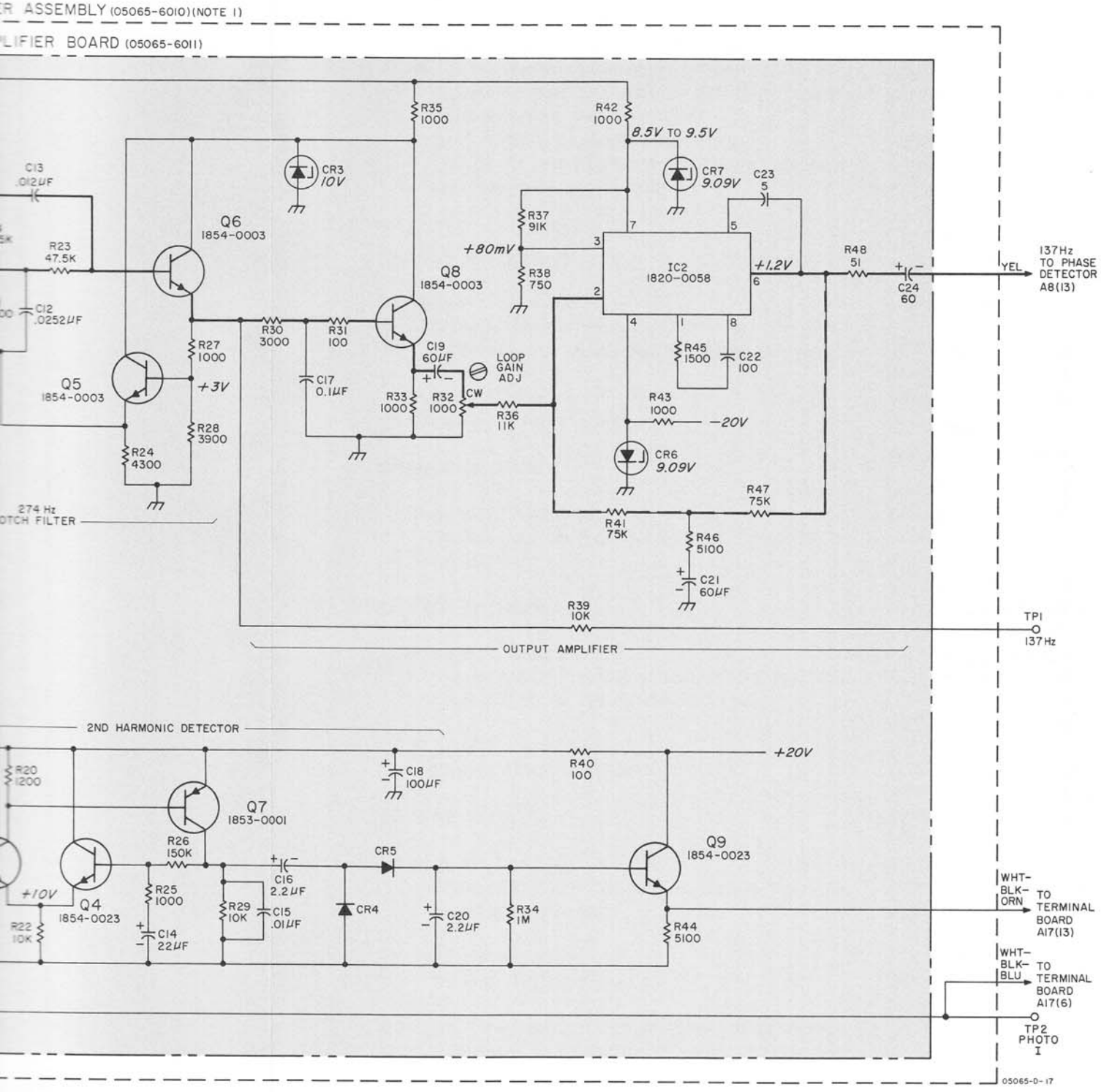


Figure 7-13. A7 AC Amplifier Schematic Diagram

CHANGE 14 (1104):

Page 6-3, Table 6-2 Replaceable Parts:
Change A1A1C34 from 1000pf to 500pf 0140-0234 C:FXD MICA 500 PF 1%; 28480; 0140-0234.
Page 8-19, Figure 8-9 Sheet 2 of 2 Schematic Diagram:
Change the value of A1A1C34 from 1000PF to 500PF
Page 6-14, Table 6-2 Replaceable Parts:
Change A11CR7 and CR8 to 1901-0049 DIODE: SILICON 50PIV; 28480 1901-0049
Page 6-18, Table 6-2 Replaceable Parts:
Change F1 and F2 FUSEHOLDER part numbers from 1400-0085 to 1400-0084.

CHANGE 15 (1220):

Page 6-7, Table 6-2:
Change A3A1R1 from 0757-0924 to 0757-0907 R:FXD FLM 200 OHMS 2% 1/8W; 28480; 0757-0907.

Page 8-25, Figure 8-11:
Change A3A1R1 to 200 ohms.

CHANGE 16 (1320):

Page 6-19, Table 6-2:
Change XA2 through XA15 from 1251-0160 to 1251-0135.

CHANGE 17 (1340):

Page 6-18, Table 6-2:
Change A15C3 from 0140-0196 to 0160-2204 C:FXD MICA 100PF 5%; 72136; RDM15F101-J3C.

Page 8-71, Figure 8-27:
Change A15C3 from 150PF to 100PF.

CHANGE 18 (1416):

Page 1-4, Table 1-3:
Change CLOCK MOVEMENT to read: 24- hour with sweep second hand.

Page 3-9, paragraph 3-21:
Replace with the following:

3-21. The Time Standard Option includes a mechanical clock movement indicating time in hours, minutes, and seconds. FAST and STOP pushbuttons on the divider module (Figure 3-10) permit setting the clock movement to the nearest second. The hour and minute adjustment is the knob located on the back of the clock movement. To set, remove the top cover; then reach in and pull out knob to engage and set the clock. Push this knob back in to release. The SYNC pushbutton allows the 5065A to be synchronized to an external clock pulse.

Page 3-9, paragraph 3-25(f):
Replace with:

When the clock pulse is synchronized, the mechanical clock in the 5065A will run in step. The set knob at the rear of the clock provides coarse adjustment of hours and minutes. The FAST and SLOW switches on the A5 module provide a way to speed up or stop the clock for adjustment to the nearest second.

Page 3-12, paragraph 3-28:
Replace "Setting the Clock" with:

3-28. Setting the Mechanical Clock

a. To mechanically set the clock, remove the top cover for access. Use the set knob at the rear of the clock; pull out to engage and set.

b. The FAST and STOP pushbuttons on A5 Assembly are accessible with the top cover removed.

10 PPS is routed to the clock with the FAST pushbutton depressed. The STOP pushbutton disconnects the clock drive.

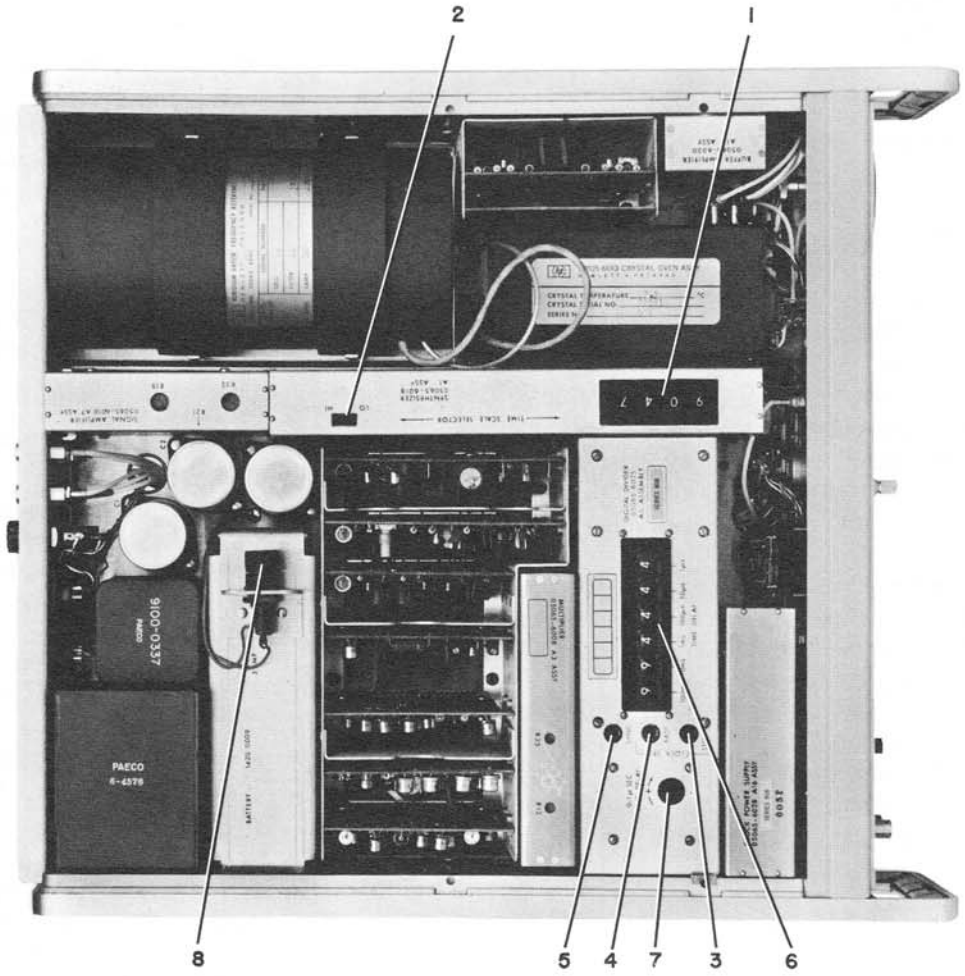
Page 3-15, Figure 3-11:
Replace Figure 3-10 with Figure 7-14.

Page 4-2, paragraph 4-17:
Replace with the following paragraph:

4-17. Additional A5 controls are the internal FAST, STOP, and SYNC switches. The FAST pushbutton speeds up clock movement by replacing the 1 PPS clock drive with 10 PPS. The STOP pushbutton shorts the 1 PPS clock drive to ground to stop the clock. To synchronize the 1 PPS output with a reference pulse, the SYNC pushbutton is depressed for at least 1-second and then released. If a sync pulse is connected to the rear SYNC INPUT jack, one reference pulse will enter the synchronizing circuits during the 1-second interval. This pulse will reset the digital divider. The output 1 PPS "tick" pulse from the 1 PPS front panel jack will then be in sync with the reference pulse.

Page 4-3, paragraph 4-18:
The sentence beginning
"The other 1 PPS input "(normally 1 PPS but 10 PPS with A5 FAST pushbutton depressed)" . . . .

Figure 7-14. Top Operating Controls



1. Synthesizer TIME CLOCK SELECTOR thumbwheel switch: selects synthesized frequency.

2. Synthesizer TIME SCALE SELECTOR HI-LO switch: used with thumbwheel switch to select synthesized frequency.

3. CLOCK SET STOP switch (Option 001 only): digital clock is stopped when switch is depressed, starts when released.

4. CLOCK SET FAST switch (Option 001 only): digital clock second hand is accelerated when switch is depressed, resumes normal operation when released.

5. Clock SYNC switch (Option 001 only): Synchronizes digital clock with an external clock when depressed; clock remains synchronized when released.

6. Clock TIME DELAY thumbwheel switch (Option 001 only): selects time delay between an external reference pulse and the internal 1 pulse-per-second clock pulse. Adjustable in decade steps from 1 μs to 1 sec.

7. 0-1 μSEC TIME DELAY control (Option 001 only): Allows continuous adjustment of clock pulse delay over any 1 μsec range.

8. Battery fuse: removed momentarily to disconnect optional standby battery from circuit for storage or shipment. Battery will remain disconnected after fuse is replaced.

Page 6-2, Figure 6-1:
Change: Panel: Left Insert; to 05065-0011. Door Panel; to 05065-0015. Standard Panel Insert; to 05065-0012. Panel Option 002 Insert; to 05065-0014.

Page 6-7, Table 6-2
Change A3A1Q9 to1854-0091 TSTR:SI NPN; 28480; 1854-0091.

CHANGE 19 (1420):

Page 6-26, Table 6-4:
Add A5B1, 05061-6085 Clock Assy: Opt. 001-003; 28480;05061-6085
Change 05065-0048 to Digital Divider 05065-0037.
Change A5,05065-6084 to Module Assy Digital Divider 05065-6025.
Add A5S1 and A5S3 SWITCH: PUSHBUTTON SPST; 82389;961 LESS HWD (both switches identical).

Page 6-27, Table 6-5:
Change A16 from 05065-6085 to 05065-6028.
Change A16A1 from 05065-6082 to 05065-6029.
Add the following components:
A16A1IC1; 1820-0313; IC; DTL RS/JK CLOCKED F/F; 28480; 1820-0313
A16A1Q11 and Q12; TSTR: SI NPN; 80131; 2N708.
A16A1CR13 and CR14; 1902-0554; DIODE BREAK-DOWN: 10V 1W; 28480; 1902-0554.

Page 6-28, Table 6-5:
Add Table 7-10 resistor parts list to A16 (R21 to R26):

Replace Digital Divider Assy A5 (sheet 1 of 3) with Figure 7-15.

Page 8-33, Figure 8-13:
Change A5, Digital Divider, Assy, from 05065-6084 to 05065-6025.

Page 8-35, Figure 8-15: Change A5 Digital Divider from 05065-6084 to 05065-6025.

Page 8-37, Figure 8-15: Change A5 Digital Divider Assy from 05065-6084 to 05065-6025.

Page 8-73, Figure 8-28:
Change A16 Digital Divider Assy from 05065-6085 to 05065-6029.
Change A16A1, 05065-6082 to 05065-6029
Replace A16A1 Schematic Diagram with Figure 7-16 A16A1 Digital Divider Schematic.

Page 8-69, Figure 8-26:
Add resistor A14R15 from the cathode of CR2 to ground (value of 5100 ohms). Change the value of A14R12 to 1000 ohms and A14R16 to 150K ohms.

Page 6-16, Table 6-2:
Add A14R15 0757-0941; R:FXD FLM 5.1K OHMS 2% 1/8W; 28480; 0757-0941.
Change A14R12 to 0757-0924 R:FXD MET FLM OHM 2% 1/8W; 28480; 0757-0924.
Change A14R16 to 0757-0976 R:FXD FLM 150K OHM 2% 1/8; 28480; 0757-0976.

Add the following Digital Clock text for LED Clock Series 1532A:

DIGITAL CLOCK THEORY OF OPERATION

General

The digital clock is a solid-state 24 hour clock with a seven segment LED (light emitting diode) display. It indicates time in hours, minutes and seconds in synchronism with the 5065A generated 1 PPS signal. Time may be set and synchronized using the HOLD/SLOW/FAST pushbuttons of the LED clock.

The required inputs which enable the lock to operate are connected to the clock by five wires. These are:

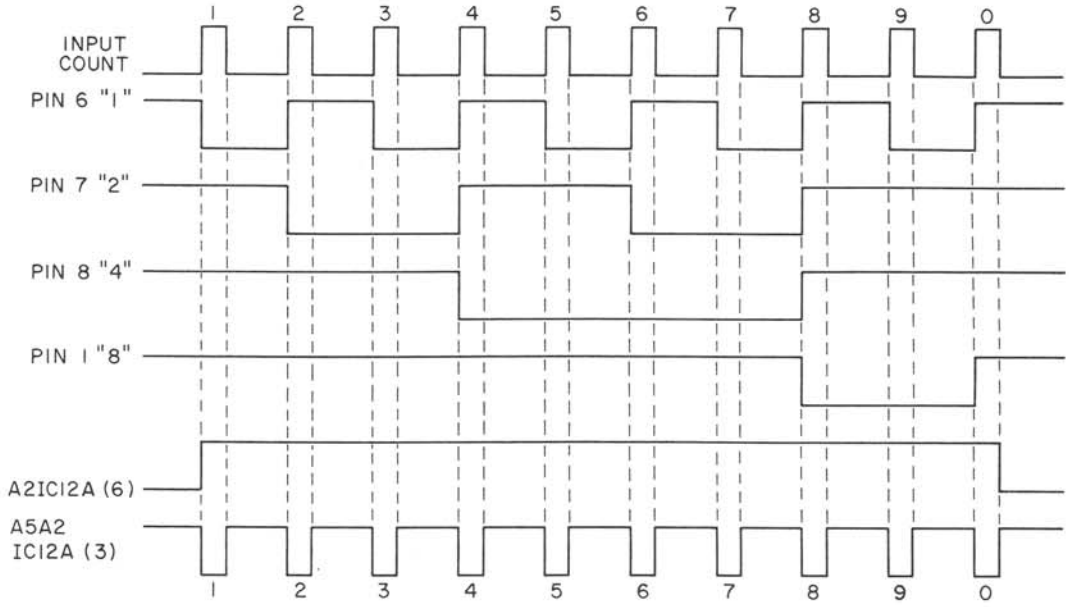
1. Unregulated +28 Vdc from the 5065A used to generate a regulated +5 Vdc and used exclusively to drive the display.

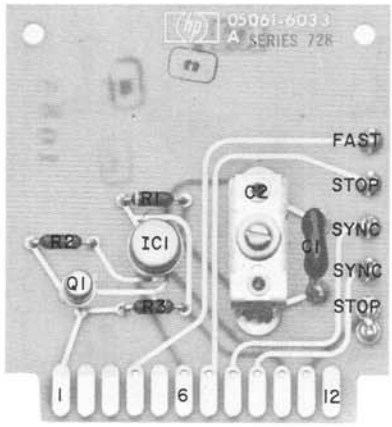
Table 7-10. A16 Resistor Parts List

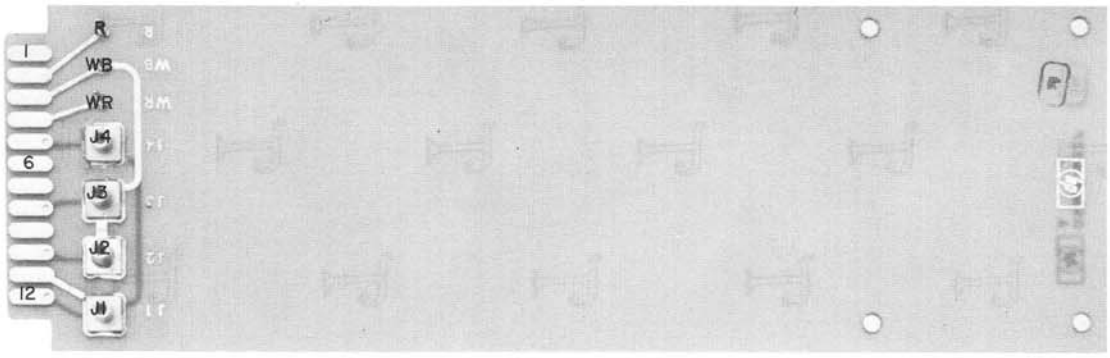
Reference Designation	HP Part Number	Qty	Description	Mfr Code	Part Number
A16A1R21	0757-0931	2	R: FXD FLM 2K OHM 2% 1/8W	28480	0757-0931
A16A1R22	0757-0931		R: FXD FLM 2K OHM 2% 1/8W	28480	0757-0931
A16A1R23	0757-0924	2	R: FXD MET FLM 1K OHM 2% 1/8W	28480	0757-0924
A16A1R24	0757-0924		R: FXD MET FLM 1K OHM 2% 1/8W	28480	0757-0924
A16A1R25	0757-0920		R: FXD FLM 680 OHM 2% 1/8W	28480	0757-0920
A16A1R26	0757-0920		R: FXD FLM 680 OHM 2% 1/8W	28480	0757-0920

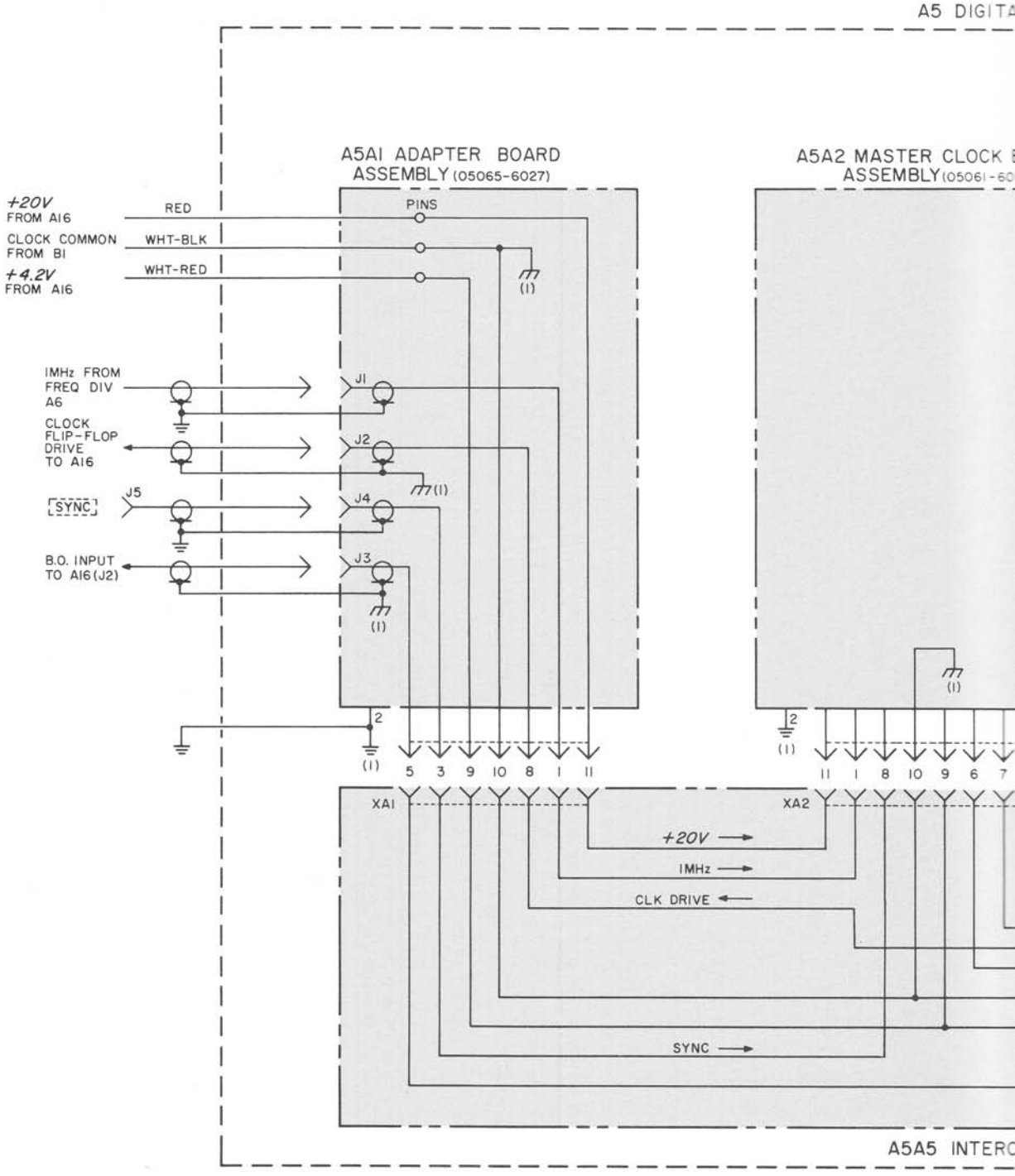
Figure 7-15
A5 DIGITAL DIVIDER ASSEMBLY (OPTION 001)

(See Page 7-39)


1 2 3 4 5 6 7 8 9 0
INPUT COUNT
PIN 6 "1"
PIN 7 "2"
PIN 8 "4"
PIN 1 "8"
A2IC12A (6)
A5A2 IC12A (3)
1 2 3 4 5 6 7 8 9 0

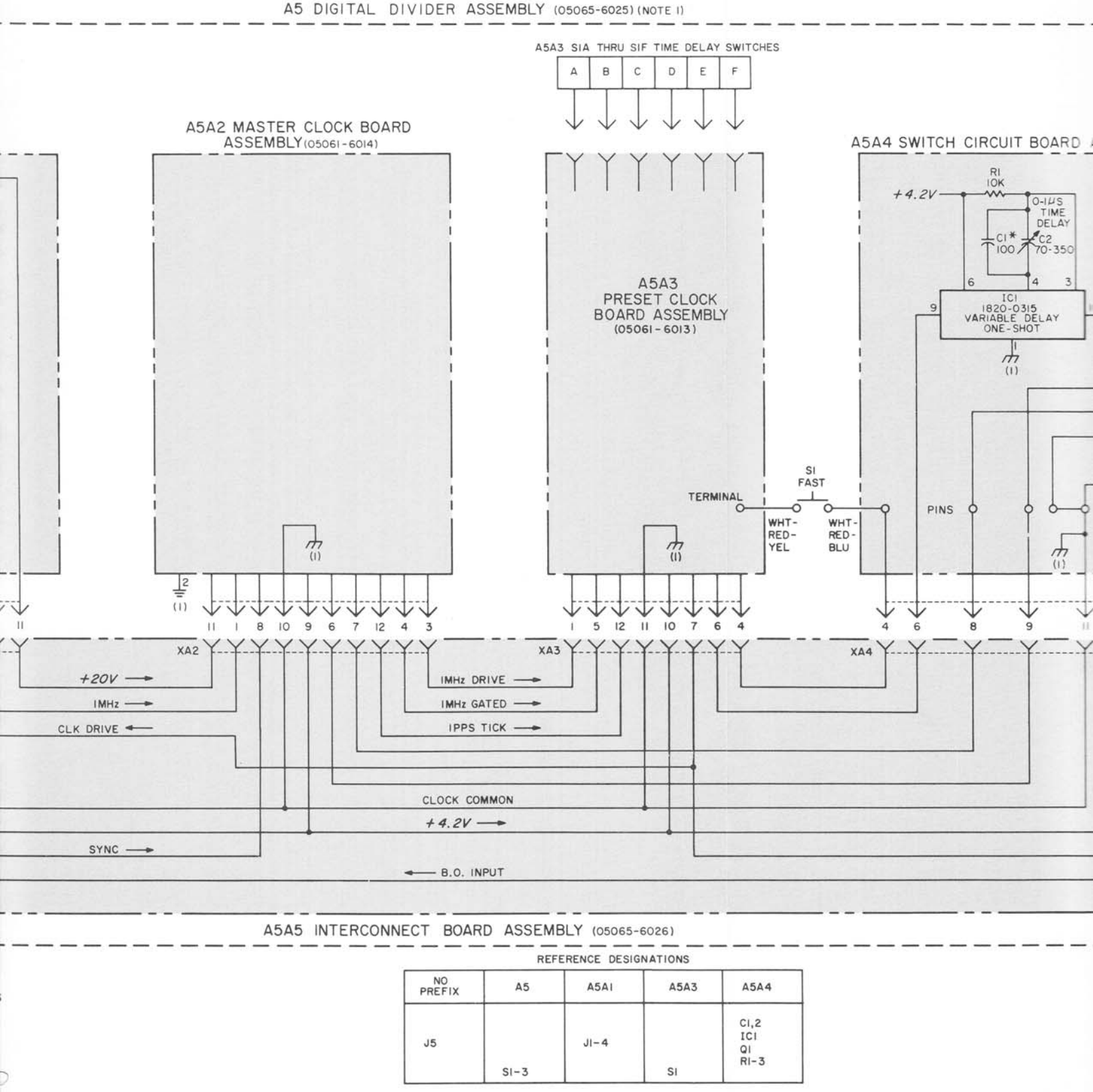

05061-6033
A SERIES 728
FAST
STOP
SYNC
SYNC
STOP
R1
R2
R3
IC1
Q1
C2
C1
1
6
12


R
WB
WR
1
6
12
J4
J3
J2
J1



NOTES

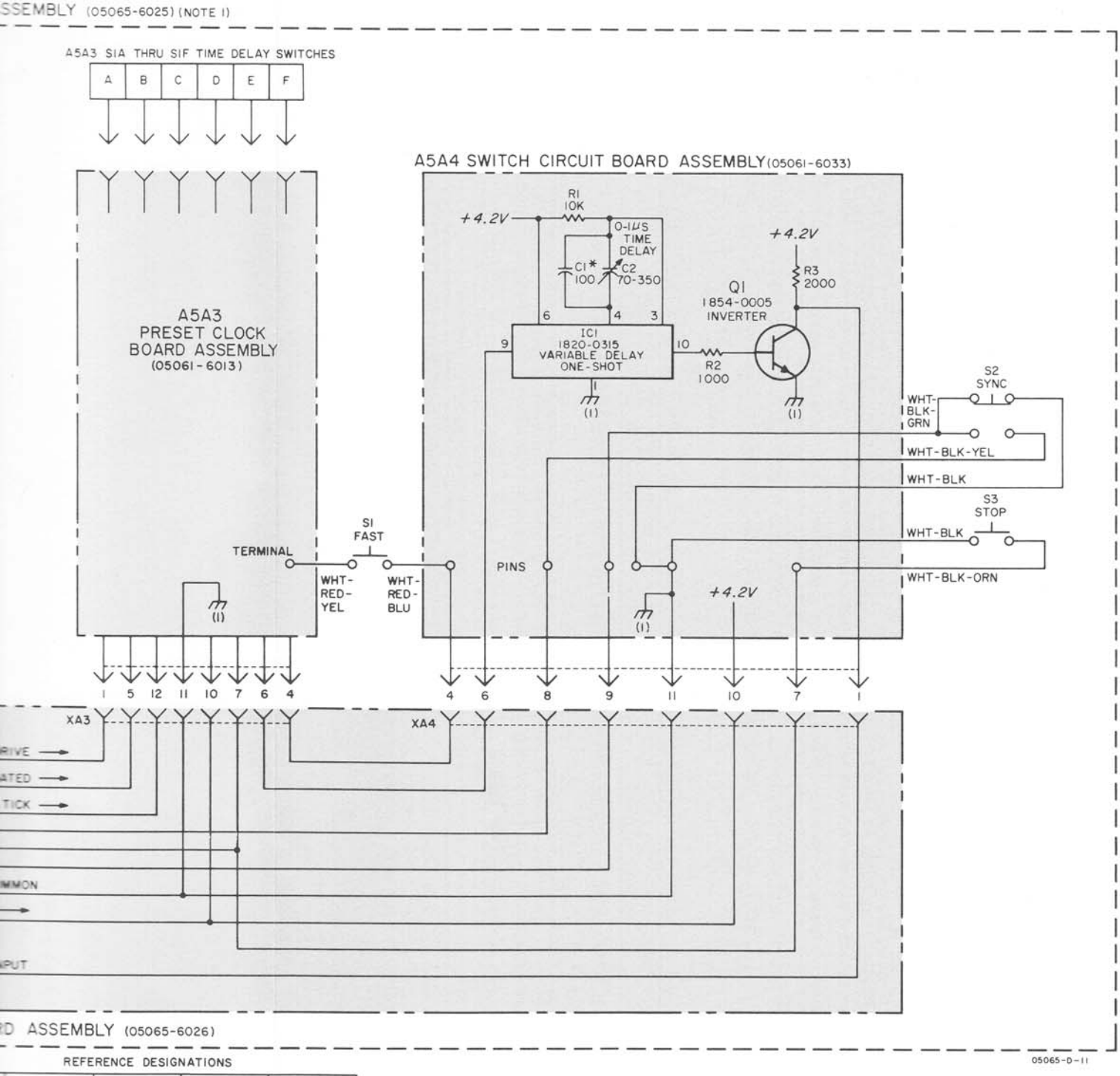
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS;
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN.



REFERENCE DESIGNATIONS

NO PREFIX	A5	A5A1	A5A3	A5A4
J5	S1-3	J1-4	S1	C1,2 IC1 Q1 R1-3

Fig



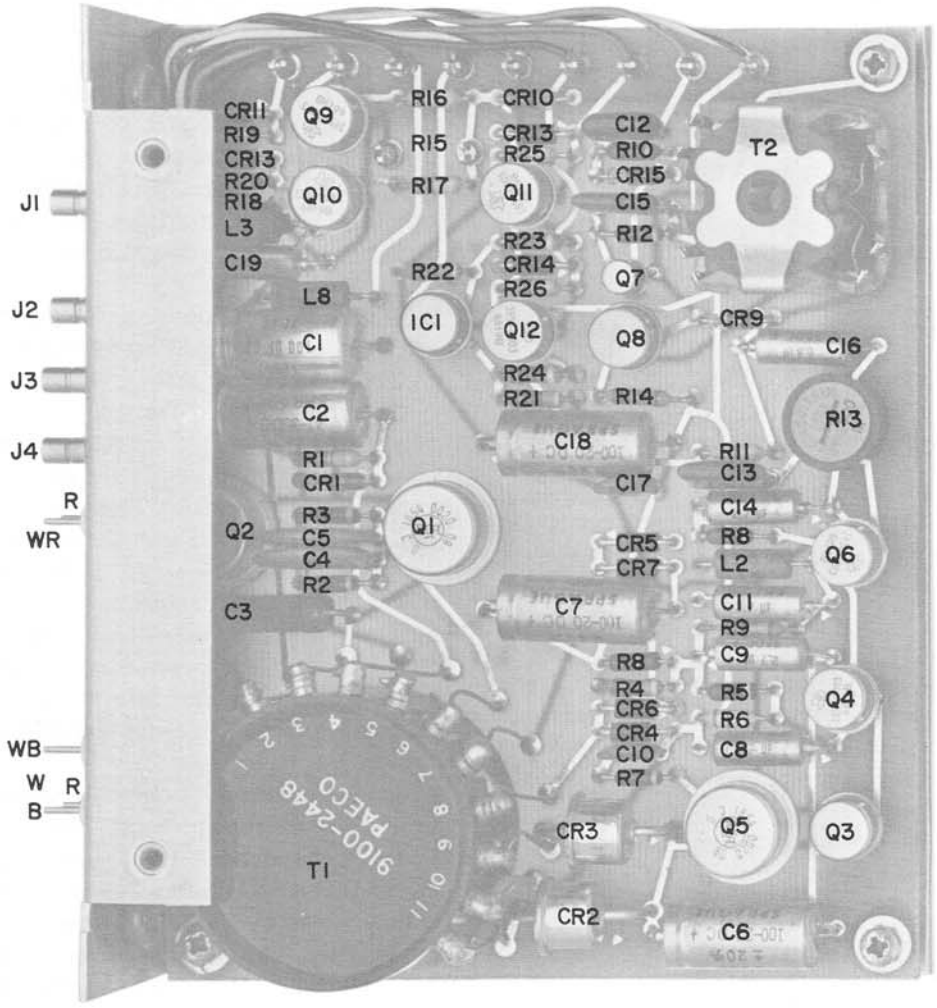
REFERENCE DESIGNATIONS

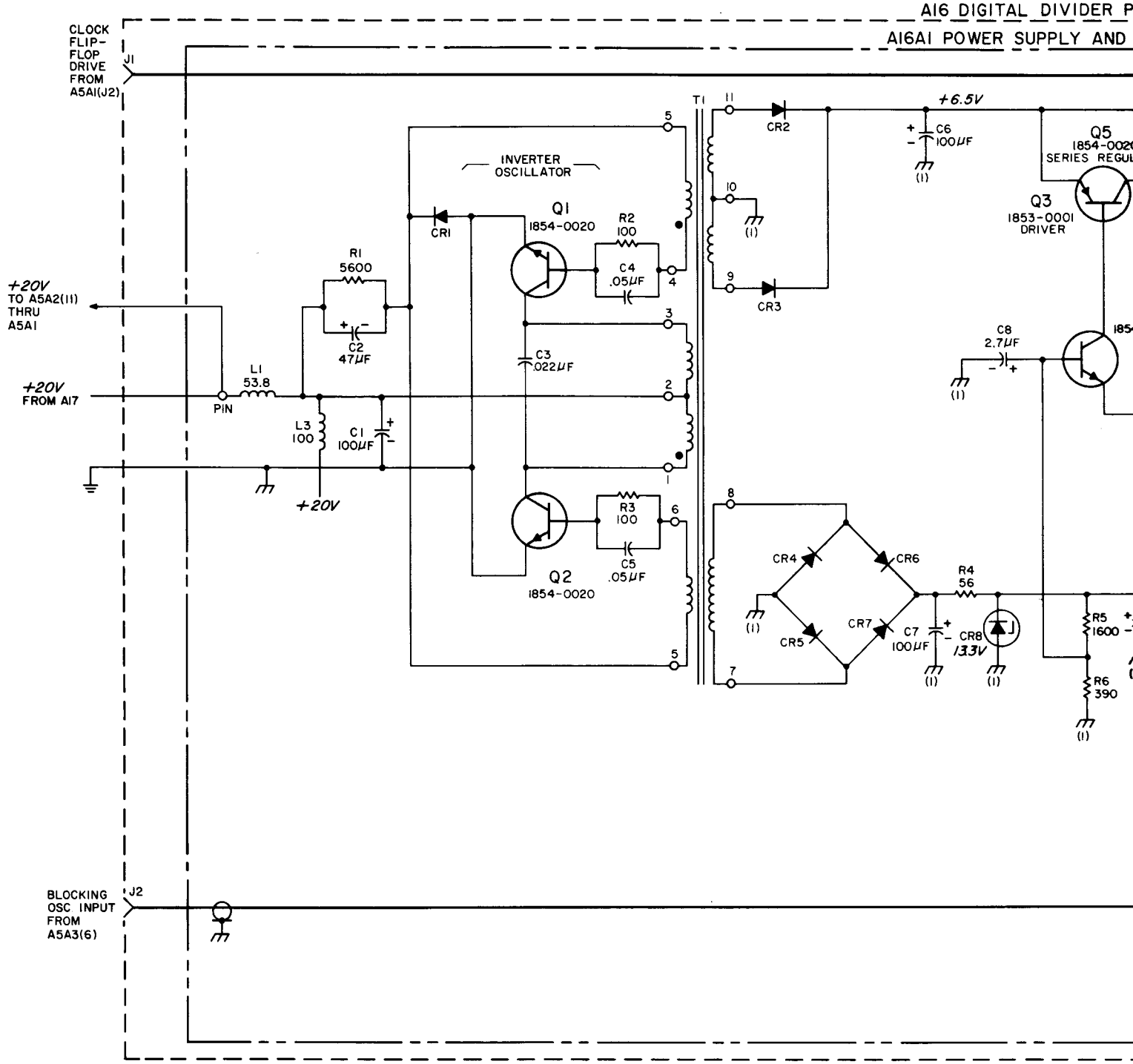
A5	A5A1	A5A3	A5A4
S1-3	J1-4	S1	C1,2 IC1 Q1 R1-3

Figure 7-15. A5 Digital Divider Assembly (Option 001)

Figure 7-16
A16 DIGITAL DIVIDER POWER SUPPLY ASSEMBLY

(See Page 7-41)


CRII
RI9
CRI3
R20
RI8
L3
CI9
Q9
Q10
RI6
RI5
RI7
CRI0
CRI3
R25
QII
R23
CRI4
R26
R22
L8
ICI
CI
C2
RI
CRI
R3
C5
C4
R2
C3
Q2
QI
Q12
R24
R21
CI8
CI2
RI0
CRI5
CI5
R12
Q7
Q8
CI7
CR5
CR7
C7
R8
R4
CR6
CR4
CIO
R7
CR3
CR2
T2
CR9
CI6
RI3
RII
CI3
CI4
R8
L2
CII
R9
C9
R5
R6
C8
Q5
C6
Q6
Q4
Q3
J1
J2
J3
J4
R
WR
WB
W
R
B
T1
9100-2448
PAECO



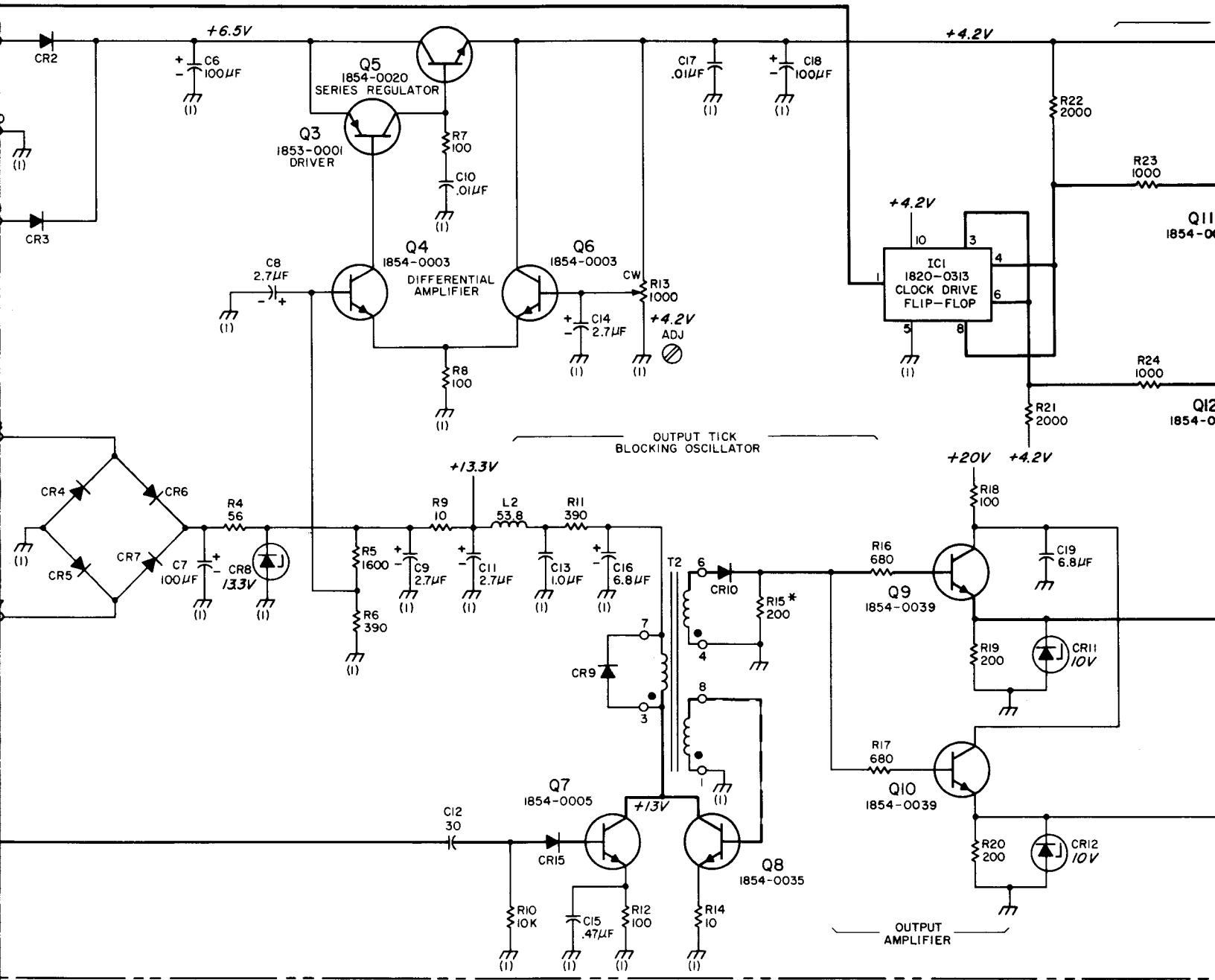
NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN

NO PREFI
J14

A16 DIGITAL DIVIDER POWER SUPPLY ASSEMBLY (05065-6028) (NOTE 1) SERIES 1104

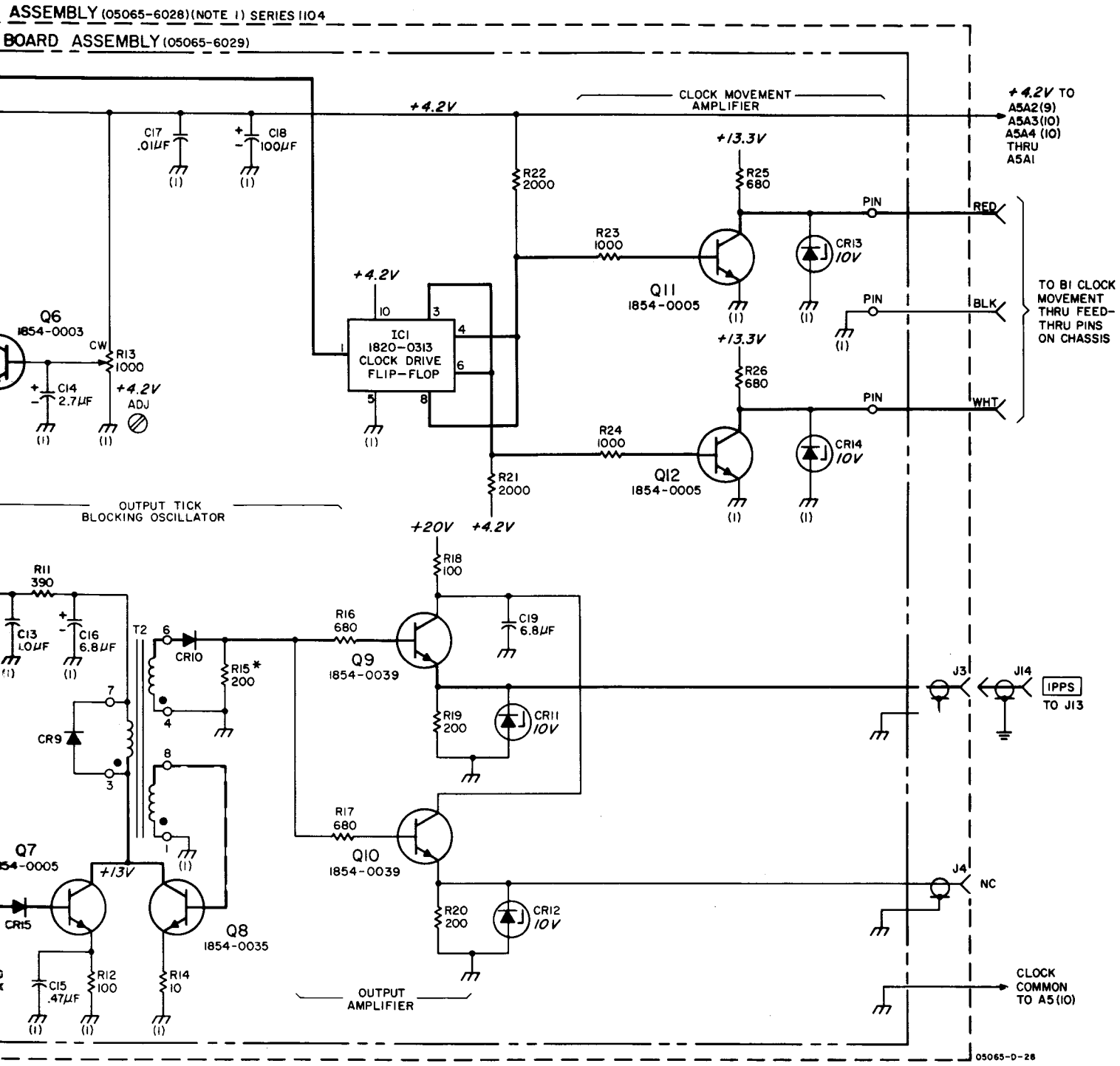
A16A1 POWER SUPPLY AND IPPS OUTPUT BOARD ASSEMBLY (05065-6029)



REFERENCE DESIGNATIONS

NO PREFIX	A16	A16A1
J14	J1-4	C1-19 CR1-15 IC1 L1-3 Q1-12 R1-26 T1,2

Figur



A16A1
C1-19
CR1-15
IC1
L1-3
Q1-12
R1-26
T1,2

Figure 7-16. A16 Digital Divider Power Supply Assembly

2. Unregulated +12 Vdc from the 5065A used exclusively to operate the CMOS circuits in the clock.
3. 1 PPS signal from the 5065A used to synchronize the clock and increment the display.
4. AC line sense signal from A2(9) turns off the display portion if instrument AC power fails or is removed. To display time, when AC power is not available, the clock front-panel STANDBY READ must be pressed.
5. 1 PPS and 12 Vdc common.Circuit ground connects to the chassis through the LED digital clock circuits.

Three circuit boards make up the A19 LED digital clock. These are:

1. A1, +5V switching regulator. This is the rear board.
2. A2, 50 Hz logic. This is the middle board.
3. A3, clock display. This is the front board.

A1, +5V Switching Regulator

This assembly is a 9 kHz to 18 kHz switching regulator which generates +5V, ±4 Vdc from the instruments' unregulated +28 Vdc input. It consists of switch Q1, voltage regulator U1, current limit circuit Q2 and input and output filter circuits.

The +28 Vdc input voltage is filtered by C1, L1, C2 and is applied to U1(8) and Q1. U1(7) output is a +5 Vdc rectangular wave signal which switches Q1 at a 9 to 18 kHz rate depending on load current and input voltage.

A reference voltage output is generated at U1(4) and is applied to U1(3). The filtered +5 Vdc output is monitored at U1(2) and any differences between U1(3) and U1(2) changes the duty-cycle of U1(7) output. The duty-cycle change adjusts Q1 on-off Times. If the +5 Vdc output tends to increase, Q1 on-time decreases which reduces the output voltage. If the +5 Vdc output tends to decrease, Q1 on-time increases which increases the output voltage.

Current limiter Q1 senses the current flow through R8. Excessive current turns Q1 on and is sensed at U1(9). This sets U1 into current-limit mode which reduces the +5 Vdc output to zero. Current limit occurs at about 450 mA. When the cause of excessive current is removed, the +5 Vdc output returns to normal.

Diode CR1 is a commutating diode which conducts L2 coil current during Q1 off-times. R1, CR8 are part of an ac sense circuit which monitors the unregulated, instrument generated dc and switches the clock display off whenever ac power is not available.

A2, 50 Hz Logic Board

The 50 Hz logic board generates the 50 Hz signal which operates the clock display. It also synchronizes the clock display advance with the instrument generated 1 PPS signal. This board also contains the ac sense circuits which turn off the clock display whenever ac power to the instrument is not available.

When power is first applied, the RC time constant of R3, C1 causes one shot M.V. U3B(13) to generate a pulse output. The pulse period is determined by the RC time constant of (R7-C3). U3B(13) output resets U3A which sets U3A(1) low and disables gate U1B. With this gate disabled, no clock pulses are gated thru U1B to U2(1).

U3B(13) one-shot output is also gated thru U5B, clocks U6B and turns on the 65 Hz free running M.V. comprised of U1D, U5D and its associated components. The 65 Hz output from U5D is gated thru U5A to the A3 clock display board U1(19). U1, on A3 clock display board, accumulates the 65 Hz pulses and generates a pulse output at 50th pulse (1 second). This pulse is used to synchronize the clock display with the instruments' 1 PPS. The 1-second clocks U3A on A2, 50 Hz logic board. U3A(1) output goes high, enables U1B and allows the 65 Hz pulses to clock U2. U2 counts to 49 which is sensed by U4C. U4C output is inverted by U4A, gated thru U4B and inverted again to a high level thru U5C. This level resets U6B and turns off free-running M.V. U1D U5D.

Accumulator U1 on A3 clock display board, has counted to 49. The instrument 1 PPS input to the 50 Hz logic board is "stretched" and level-changed thru Q2 and clocks U6A. U6A is a one-shot M.V. whose 75 usec period is determined by R6, C2 RC time-constant. U6A(1) output is gated thru U5A to A3 clock display board U1, as the 50th cycle. The clock display then advances one second. The U6A output pulse is delayed by R8-C4, gated thru U5B(5) and clocks U6B which starts free-running M.V. U1D, U5D.

The delay circuit R8, C4 provides a time delay between the 1 PPS generated 50th cycle, which causes the display to increment 1 second, and the start of the next free running M.V. cycle, which enables U1 on A3 clock display board to count to 49.

A3, Clock Display Board

The clock display board consists of a MOS clock chip, a transistor array, a buffer amplifier array, four driver transistors and six LED displays. This assembly's function is to accumulate and display time-of-day in synchronism with the instruments' 1 PPS signal.

The MOS clock circuit U1 operates from the 50 Hz input from A2 50 Hz logic board. U1 divides the 50 Hz signal by 50 and generates a 1 PPS output at pin 20 which is used to synchronize the display to the instrument 1 PPS signal.

Counter stages with U1 divide the input 50 Hz signal and generate the hours, minutes, and seconds outputs for the LED displays.

The time display signals from U1 are comprised of two parts:

1. The digit enable signal.
2. The multiplexed 7-segment signal.

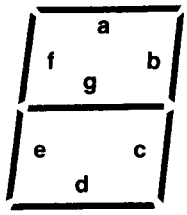
The digits enable signals from U1 are:

Pin 23: tens-of-hours.
Pin 24: units-of-hours.
Pin 25: tens-of-minutes.
Pin 26: units-of-minutes.
Pin 21: tens-of-seconds.
Pin 22: units-of-seconds.

These signals enable the LED displays through U3 gates, and allow the multiplexed 7 segments outputs to turn-on the correct display segment.

The multiplexed 7 segment signals from U1 are (see Figure __ for "segments"):

Pin 6: for segment a.
Pin 7: for segment b.
Pin 8: for segment c.
Pin 9: for segment d.
Pin 10: for segment e.
Pin 11: for segment f.
Pin 12: for segment g.



These "segment enabling signals" are buffered through U2 stages and applied to the LED displays. Thus, the segments of an individual number display are enabled by outputs from U1(6 to 12) while the number itself is turned on by one of the U1 (21 to 26) outputs.

MAINTENANCE

General

The A19 LED Digital Clock Assembly has no adjustments and requires no periodic maintenance. Should repair be necessary, the unit may be removed and operated on the bench while remaining connected to the instrument. When operating in this manner, however, the clock chassis or circuit common **must be connected to the instrument chassis** with a CLIP LEAD OR JUMPER WIRE. The following paragraphs describe assembly removal, fault finding procedures for the clock system, and troubleshooting information for the individual circuits.

NOTE

Most of the circuits on the 50 Hz LOGIC and CLOCK DISPLAY assemblies are CMOS. Use high impedance tet equipment when checking signals. Precautions should be taken when removing or replacing these circuits to prevent damage from static charges.

Repairs

Before repairs are attempted:

a. Momentarily set front panel DIVIDER MODE switch to START.
b. Check CIRCUIT CHECK meter in 1 MHz position for reading of approximately 40. If not, troubleshoot A6 assembly.
c. Check front panel 1 PPS output. If not present, troubleshoot A5 assembly.
d. If the display is not lit, press STANDBY DISPLAY switch. If display lights and operates normally, the instrument is not operating from AC power. This condition is normal. If the display does not light when the STANDBY DISPLAY switch is pressed, perform troubleshooting procedures.
e. Read LED Digital Clock Theory of Operation.

A19 Assembly Removal

Prior to removing or reinstalling the LED Digital Clock, all operating power must be removed. Wire and cable

length to the clock panel or clock rear board is sufficient to enable removal of the clock without disconnecting these wires or the cable. The clock should be placed on a pad or cloth to minimize scratch damage or shorting of circuit traces.

To remove the clock:

a. Remove all operating power.

b. Remove the instrument top cover. In Option 003 disable the internal standby battery.

c. Use a 5/16" wrench and remove two 5/16" nuts which secure the clock to the instrument front panel. Retain the nuts for reinstallation. The bottom of the clock is retained in place by a third nut which must also be removed.

d. Press firmly at the bottom-rear then at the top-rear of the clock until it is loose.

e. Gradually remove the clock. Gently pull the connected wires and cable forward and set the clock on the work surface.

f. Before applying operating power ensure that the exposed LED Clock boards and wires are not in contact with any metal objects or surfaces. Reapply operating power.

g. To reinstall the LED clock, remove all operating power. In Option 003, disable the internal standby battery.

h. Do steps b to e in reverse order. (See Note.)

NOTE

While installing the clock into the instrument front panel, check that wires are not pinched by screws or metal work. Position the wires for a neat appearance after installation.

i. When clock is reinstalled, reapply power and set time as described in replacement paragraph for page 3-12, paragraph 3-38 of your 5065A Operating and Service Manual.

TROUBLESHOOTING

General

Each of the circuit boards in this assembly perform a specific function, requiring only 1 of 2 inputs to generate its output. These can easily be checked without disassembling the clock.

Procedures in this section describe fault isolation to the circuit board level, disassembly of the clock, and troubleshooting information for each of the three circuits.

Clock System Troubleshooting

To perform the following tests the clock must be removed from the instrument and connected as described in A19 ASSEMBLY REMOVAL of this change sheet.

A1 Power Supply Check

NOTE

All voltages measured with respect to instrument chassis.

a. Measure voltages indicated below. Be sure clock chassis is grounded to instrument chassis.

VOLTAGE	LOCATION
+26 ±4V dc	**A16A1(3)**
+12 ±2V dc	**A16A1(R)**
+5 ±.2V dc	**A16A1(4)**

b. If the +26 or +12 volt supplies are out of tolerance, troubleshoot the source of these voltages. If the +5V supply is out of tolerance, remove the connection between A1(4) and A2(4) and measure the voltage again. If voltage now is correct, go to step b(2).

(1) If voltage remains out of tolerance, troubleshoot A1, 5V regulator assembly. See clock repair and disassembly, step 1 and "Circuit Board Troubleshooting", step 1.

(2) If voltage is now correct it indicates a short or low impedance on 5V line or defective current-limit circuit: troubleshoot 5V line and circuits on A3 which use 5V. If these are OK, check current-limit circuit of A1Q2.

NOTE

An external 5 V can be used in place of A1 output.

c. Check for +1V, 150 nsec, 1 PPS signal at A1(W). Be sure clock chassis is grounded to instrument chassis. If pulse not present, troubleshoot A16 Assembly.

A3 Clock Display Check

a. If display is not lit go to "Display not lit" step 2. If display is lit but not functioning correctly continue:
1. Check waveform at A3(2). It should be as shown on schematic.

2. If correct, go to item 5 of this paragraph. If incorrect or not present, cut 1 PPS wire between A3(1) and A2.
3. Press and release HOLD pushbutton. Momentarily connect a clip lead from the +12V supply (A1(R)) to where 1 PPS wire (cut in previous step) connects to A2 assembly.
4. Recheck waveform at A3(2). If correct, replace A3U1. If incorrect troubleshoot A2. See "Clock Repair and Disassembly" step 3 and "Circuit Board Troubleshooting", step 3.
5. Connect a counter, set to totalize (manual gate open) to A3(2).
6. Unplug the white wire (which connects the clock assembly to the instrument chassis) at the instrument chassis.
7. Reset counter to zero and momentarily reconnect white wire removed in step 6. Disconnect white wire as soon as the counter starts counting.
8. Counter should read 51 pulses or multiplies of 51 (depending on how quickly the white wire was disconnected). If the counter reads incorrectly troubleshoot A2. See "Clock Repair and Disassembly", step 3 and "Circuit Board Troubleshooting", step 3.
9. Check A3(1) for a 1 PPS square wave. If not present, check for +12V at A3(11). If +12V is present, replace A3U1. If 1 PPS is present, troubleshoot A3, See "Clock Repair and Disassembly", step 2 and "Circuit Board Troubleshooting", step 2.

b. Display Not Lit

1. Check voltage at A3(5). It should be a few tenths-of-a-volt less than the voltage at A1(4). If incorrect, troubleshoot "AC SENSE" CIRCUIT ON A2. See "Clock Repair and Disassembly" step 3 and "Circuit Board Troubleshooting", step 3.
2. Check +12V input at A3(11). It should be the same as measured at A1(R). If not, check continuity of +12V line from A1 to A3.
3. Substitute a new LED in one of the display positions.
4. Trouble is in U1, 2 or 3. Check for switching waveforms at U1(6-12) and (21-26). Check for switching waveforms at U2 and U3 outputs. See schematic for typical waveforms.

A2 50 Hz Logic Check

Troubleshooting checks to this point have isolated most problems to the failed circuit board. Problems of a more subtle nature such as clock not keeping correct time, or display not synchronized to the instrument's 1 PPS output signal, are the type of problems associated with the 50 Hz logic board.

Clock Repair and Disassembly

1. To troubleshoot A1 5V regulator board it is not necessary to disassemble the clock. The board may be removed when making repairs, if soldering is required on the backside of the board.
2. To troubleshoot A3 display assembly remove three nuts which secure the circuit boards to the front panel assembly. Remove STANDBY DISPLAY switch from front panel. Remove Clock Circuit Board Assembly from front panel assembly. Remove six spacers from between boards. Reconnect all wires. Be sure to connect clock circuit ground (pads under spacers) to instrument chassis.
3. To troubleshoot A2 50 Hz LOGIC do step 2 above, but do not connect wires. Unsolder A3 from A2. Connect only the black and red wires (from A1 to instrument). Also connect clock circuit ground (pads under spacers) to instrument chassis.

CIRCUIT BOARD TROUBLESHOOTING

A1 Power Supply

Since this circuit contains only four active components, it is relatively easy to troubleshoot. With power disconnected check Q1, Q2, CR1 and capacitors. If these are good, trouble is probably in A1U1.

A3 Clock Display

U1 accumulates time, and drives the LED displays thru U2, U3 and transistors Q1-6. To troubleshoot, observe that switching signal originating at U1(6-12) is reaching U3 outputs, and signal at U1(21-26) is reaching collectors of Q1-6. LEDs can be checked by substitution. If all signals are correct trouble is in U1.

A2 50 Hz Logic

a. Momentarily press HOLD button.
b. Momentarily connect a jumper from +12V supply to U3(3). This resets the counters and enables

input one-shot U6A. Circuit cannot operate until this is done.

NOTE

When viewing A2 waveforms it is helpful to synchronize oscilloscope from front panel 1 PPS output.

c. If clock time is incorrect or out of sync:

1. Check 65 Hz oscillator (U6B, U1D, U5D), 49-counter (U2), 49-sense, (U4C, U4A) and amplifier circuits (U2, 4, 5).

2. Check operation of U3A and U3B (press HOLD trigger U3A and reset U3B. Connect +12V to U3(3) to operate U3A.

d. If there is no output from A3, check 1 PPS signal path thru U5A.

NOTE

U6A is enabled by a high level (12V) at U6(5). If this level is incorrect repeat steps a and b. If level does not change, trouble is in 49-count or sense circuits (U2, U4C, U4A).

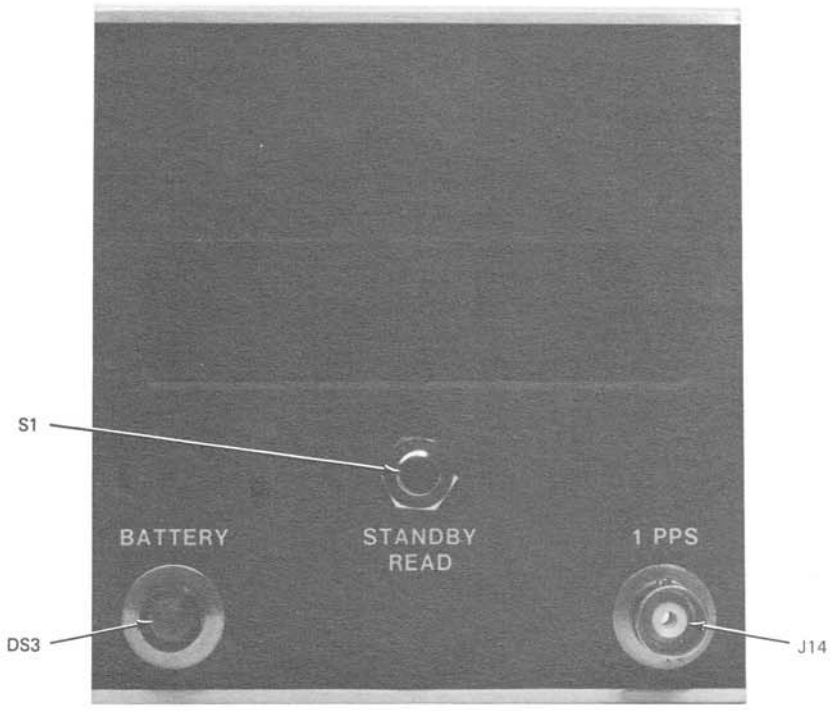
Table 1. A19 SERIES 1532 Digital Clock Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A19	05061-6120	1	CLOCK ASSEMBLY, LED FOR OPT 001	28480	05061-6120
A1	05061-6117	1	BOARD ASSEMBLY, REGULATOR	28480	05061-6117
A2	05061-6116	1	BOARD ASSEMBLY, 50 HZ LOGIC	28480	05061-6116
A3	05061-6115	1	BOARD ASSEMBLY, DISPLAY	28480	05061-6115
J13	1250-0102	1	CONNECTOR-RF BNC FEM SGL HOLE FR	28480	1250-0102
S1	3101-0052	1	SWITCH-PB SPST NO MOM .25A 30VAC	82389	961
S2	3101-0557	3	SWITCH-PB SPST NO MOM .5A 120VAC	09353	8631-E
S3	3101-0557		SWITCH-PB SPST NO MOM .5A 120VAC	09353	8631-E
S4	3101-0557		SWITCH-PB SPST NO MOM .5A 120VAC	09353	8631-E
			MISCELLANEOUS		
	1200-0063	3	CONNECTOR-SGL CONT SKT (FOR GOLD-POST CONNECTORS)	28480	1200-0063
	5020-0176	3	INSULATOR FOR SNAP-ON PINS (FOR GOLD-POST CONNECTORS)	28480	5020-0176
	05061-0078	1	BRACKET, SWITCH	28480	05061-0078
	05061-2118	1	PANEL, CENTER	28480	05061-2118
	05061-2120	1	PLATE, CENTER	28480	05061-2120
	05062-20162	1	WINDOW, DISPLAY	28480	05062-20162
A19	05061-6119	1	CLOCK ASSEMBLY, LED FOR OPT 003	28480	05061-6119
A1	05061-6117		BOARD ASSEMBLY, REGULATOR	28480	05061-6117
A2	05061-6116		BOARD ASSEMBLY, 50 HZ, LOGIC	28480	05061-6116
A3	05061-6115		BOARD ASSEMBLY, DISPLAY	28480	05061-6115
DS3	2140-0025	1	LAMP-INCAND T-1-3/4 BULB 28V	28480	2140-0025
	1450-0114	1	LIGHT-IND LAMPHOLDER AMB TP LENS	07137	RDL-B3-F3-000
J13	1250-0102		CONNECTOR-RF BNC FEM SGL HOLE FR	28480	1250-0102
S1	3101-0052		SWITCH-PB SPST NO MOM .25A 30VAC	82389	961
S2	3101-0557		SWITCH-PB SPST NO MOM .5A 120VAC	09353	8631-E
S3	3101-0557		SWITCH-PB SPST NO MOM .5A 120VAC	09353	8631-E
S4	3101-0557		SWITCH-PB SPST NO MOM .5A 120VAC	09353	8631-E
			MISCELLANEOUS		
	1200-0063		CONNECTOR-SGL CONT SKT (FOR GOLD-POST CONNECTORS)	28480	1200-0063
	5020-0176		INSULATOR FOR SNAP-ON PINS (FOR GOLD-POST CONNECTORS)	28480	5020-0176
	05061-0078		BRACKET, SWITCH	28480	05061-0078
	05061-2119	1	PANEL, CENTER	28480	05061-2119
	05061-2120		PLATE, CENTER	28480	05061-2120
	05062-20162		WINDOW, DISPLAY	28480	05062-20162
A1	05061-6117		BOARD ASSEMBLY, +5V REGULATOR	28480	05061-6117
A1C1	0160-3879	3	CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A1C2	0180-0141	2	CAPACITOR-FXD; 50UF+75-10% 50VDC AL	56289	30D506G050DD2
A1C3	0180-1743	2	CAPACITOR-FXD; .1UF+-10% 35VDC TA-SOLID	56289	150D104X9035A2
A1C4	0180-1743		CAPACITOR-FXD; .1UF+-10% 35VDC TA-SOLID	56289	150D104X9035A2
A1C5	0180-0098	1	CAPACITOR-FXD; 100UF+-20% 20VDC TA	56289	150D107X0020S2
A1C6	0160-2204	1	CAPACITOR-FXD 100PF +-5% 300WVDC MICA	28480	0160-2204
A1C7	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A1C8	0180-0141		CAPACITOR-FXD; 50UF+75-10% 50VDC AL	56289	30D506G050DD2
A1CR1	1901-0693	1	DIODE-PWR RECT 1N4934 100V 1A 200NS	04713	1N4934
A1L1	9140-0237	1	COIL-FXD MOLDED RF CHOKE 200UH 5%	24226	15/203
A1L2	9100-0536	1	COIL-FXD NON-MOLDED RF CHOKE 1.5MH 8%	28480	9100-0536
A1Q1	1853-0012	1	TRANSISTOR PNP 2N2904A SI TO-5 PD=600MW	01295	2N2904A
A1Q2	1854-0215	3	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	SPS 3611
A1R1	0757-0928	2	RESISTOR 1.5K 2% .125W F TC=0+-100	24546	C4-1/8-TO-1501-G
A1R2	0757-0935	1	RESISTOR 3K 2% .125W F TC=0+-100	24546	C4-1/8-TO-3001-G
A1R3	0683-3605	1	RESISTOR 36 5% .25W FC TC=-400/+500	01121	CB3605
A1R4	0683-1055	2	RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055
A1R5	0757-0928		RESISTOR 1.5K 2% .125W F TC=0+-100	24546	C4-1/8-TO-1501-G
A1R6	0757-0937	1	RESISTOR 3.6K 2% .125W F TC=0+-100	24546	C4-1/8-TO-3601-G
A1R7	0757-0924	4	RESISTOR 1K 2% .125W F TC=0+-100	24546	C4-1/8-TO-1001-G
A1R8	0698-8177	1	RESISTOR 1.5 5% .25W F TC=0+-100	11502	TF07-1/4-TO-1R5-J
A1R9	0757-0924		RESISTOR 1K 2% .125W F TC=0+-100	24546	C4-1/8-TO-1001-G
A1U1	1820-0196	1	IC RGLTR	07263	723HC

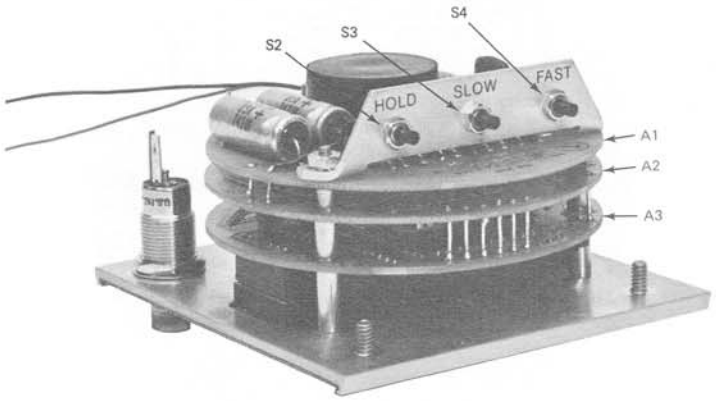
See introduction to this section for ordering information

Table 1. A19 SERIES 1532 Digital Clock Replaceable Parts (Continued)

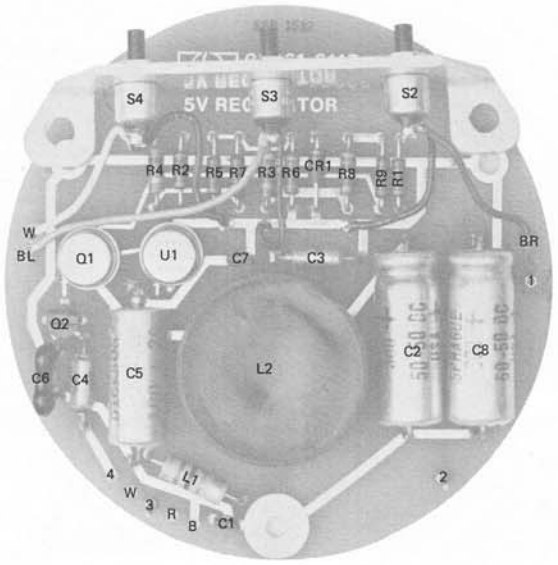
Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2	05061-6116		BOARD ASSEMBLY, 50 HZ, LOGIC	28480	05061-6116
A2C1	0160-3878	4	CAPACITOR-FXD 1000PF +-20% 100WVDC CER	28480	0160-3878
A2C2	0160-3873		CAPACITOR-FXD 1000PF +-20% 100WVDC CER	28480	0160-3873
A2C3	0160-3878		CAPACITOR-FXD 1000PF +-20% 100WVDC CER	28480	0160-3878
A2C4	0160-3873		CAPACITOR-FXD 1000PF +-20% 100WVDC CER	28480	0160-3873
A2C5	0160-0247	1	CAPACITOR-FXD .01UF +-5% 200WVDC POLYE	56289	292P10352
A2CR1	1902-3234	1	DIODE-ZNR 19.6V 5% DO-7 PD=.4W TC=+.073%	04713	SZ 10939-266
A2Q1	1854-0215		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	SPS 3611
A2Q2	1854-0215		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	SPS 3611
A2Q3	1853-0036	7	TRANSISTOR PNP SIL PD=310MW FT=250?HZ	04713	SPS-3612
A2R1	0757-0924		RESISTOR 1K 2% .125W F TC=0+-100	24546	C4-1/8-T0-1001-G
A2R2	0757-0948	2	RESISTOR 10K 2% .125W F TC=0+-100	24546	C4-1/8-T0-1002-G
A2R3	0683-1055		RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055
A2R4	0757-0955	2	RESISTOR 20K 2% .125W F TC=0+-100	24546	C4-1/8-T0-2002-G
A2R5	0757-0950	1	RESISTOR 12K 2% .125W F TC=0+-100	24546	C4-1/8-T0-1202-G
A2R6	0757-0969	1	RESISTOR 75K 2% .125W F TC=0+-100	24546	C4-1/8-T0-7502-G
A2R7	0757-0945	1	RESISTOR 7.5K 2% .125W F TC=0+-100	24546	C4-1/8-T0-7501-G
A2R8	0757-0955		RESISTOR 20K 2% .125W F TC=0+-100	24546	C4-1/8-T0-2002-G
A2R9	0683-1555	1	RESISTOR 1.5M 5% .25W FC TC=-900/+1100	01121	CB1555
A2R10	0757-0485	1	RESISTOR 681K 1% .125W F TC=0+-100	24546	NA4
A2R11	0757-0963	1	RESISTOR 43K 2% .125W F TC=0+-100	24546	C4-1/8-T0-4302-G
A2R12	0757-0948		RESISTOR 10K 2% .125W F TC=0+-100	24546	C4-1/8-T0-1002-G
A2R13	0757-0524		RESISTOR 1K 2% .125W F TC=0+-100	24546	C4-1/8-T0-1001-G
A2R14	0757-0905	1	RESISTOR 160 2% .125W F TC=0+-100	24546	C4-1/8-T0-161-G
A2U1	1820-0949	1	IC CD4011AE GATE	02735	CD4011AE
A2U2	1820-0936	1	IC CD4024AE COUNTER	02735	CD4024AE
A2U3	1820-0939	2	IC CD4013AE FLIP-FLOP	02735	CD4013AE
A2U4	1820-0943	1	IC CD4023AE GATE	02735	CD4023AE
A2U5	1820-0946	1	IC CD4001AE GATE	02735	CD4001AE
A2U6	1820-0939		IC CD4013AE FLIP-FLOP	02735	CD4013AE
A3	05061-61152		BOARD ASSEMBLY, DISPLAY	28480	05061-61152
A3C1	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3DS1	1990-0452	6	DISPLAY NUM SEG 1 CHAR .3 IN HIGH	28480	1990-0452
A3DS2	1990-0452		DISPLAY NUM SEG 1 CHAR .3 IN HIGH	28480	1990-0452
A3DS3	1990-0452		DISPLAY NUM SEG 1 CHAR .3 IN HIGH	28480	1990-0452
A3DS4	1990-0452		DISPLAY NUM SEG 1 CHAR .3 IN HIGH	28480	1990-0452
A3DS5	1990-0452		DISPLAY NUM SEG 1 CHAR .3 IN HIGH	28480	1990-0452
A3DS6	1990-0452		DISPLAY NUM SEG 1 CHAR .3 IN HIGH	28480	1990-0452
A3Q1	1853-0036		TRANSISTOR PNP SIL PD=310MW FT=250?HZ	04713	SPS-3612
A3Q2	1853-0036		TRANSISTOR PNP SIL PD=310MW FT=250?HZ	04713	SPS-3612
A3Q3	1853-0036		TRANSISTOR PNP SIL PD=310MW FT=250?HZ	04713	SPS-3612
A3Q4	1853-0036		TRANSISTOR PNP SIL PD=310MW FT=250?HZ	04713	SPS-3612
A3Q5	1853-0036		TRANSISTOR PNP SIL PD=310MW FT=250?HZ	04713	SPS-3612
A3Q6	1853-0036		TRANSISTOR PNP SIL PD=310MW FT=250?HZ	04713	SPS-3612
A3R1	0698-7964	1	RESISTOR 100K 5% .125W CC TC=0+-250	01121	BB1045
A3R2	0698-5180	7	RESISTOR 2K 5% .125W CC TC=0+882	01121	BB2025
A3R3	0698-5180		RESISTOR 2K 5% .125W CC TC=0+882	01121	BB2025
A3R4	0698-5180		RESISTOR 2K 5% .125W CC TC=0+882	01121	BB2025
A3R5	0698-5180		RESISTOR 2K 5% .125W CC TC=0+882	01121	BB2025
A3R6	0698-5180		RESISTOR 2K 5% .125W CC TC=0+882	01121	BB2025
A3R7	0698-5180		RESISTOR 2K 5% .125W CC TC=0+882	01121	BB2025
A3R8	0698-5180		RESISTOR 2K 5% .125W CC TC=0+882	01121	BB2025
A3R9	0698-4130	7	RESISTOR 39 5% .125W CC TC=0+588	01121	BB3905
A3R10	0698-4130		RESISTOR 39 5% .125W CC TC=0+588	01121	BB3905
A3R11	0698-4130		RESISTOR 39 5% .125W CC TC=0+588	01121	BB3905
A3R12	0698-4130		RESISTOR 39 5% .125W CC TC=0+588	01121	BB3905
A3R13	0698-4130		RESISTOR 39 5% .125W CC TC=0+588	01121	BB3905
A3R14	0698-4130		RESISTOR 39 5% .125W CC TC=0+588	01121	BB3905
A3R15	0698-4130		RESISTOR 39 5% .125W CC TC=0+588	01121	BB3905
A3RP1	1810-0055	1	NETWORK-RES 9-PIN-SIP .15-PIN SPCG	28480	1810-0055
A3RP2	1810-0151	1	NETWORK-RES 7-PIN-SIP .15-PIN-SPCG	28480	1810-0151
A3U1	1826-1364	1	IC MM5313N DIGITAL	27014	MM5313N
A3U2	1858-0023	1	IC CA3081 XSTR ARRAY	02735	CA3081
A3U3	1820-1146	1	IC CD4050AE BUFFER	02735	CD4050AE
A3XDS1	1200-0496	6	SOCKET, IC 16-PIN	01295	OBD
A3XDS2	1200-0496		SOCKET, IC 16-PIN	01295	OBD
A3XDS3	1200-0496		SOCKET, IC 16-PIN	01295	OBD
A3XDS4	1200-0496		SOCKET, IC 16-PIN	01295	OBD
A3XDS5	1200-0496		SOCKET, IC 16-PIN	01295	OBD
A3XDS6	1200-0496		SOCKET, IC 16-PIN	01295	OBD



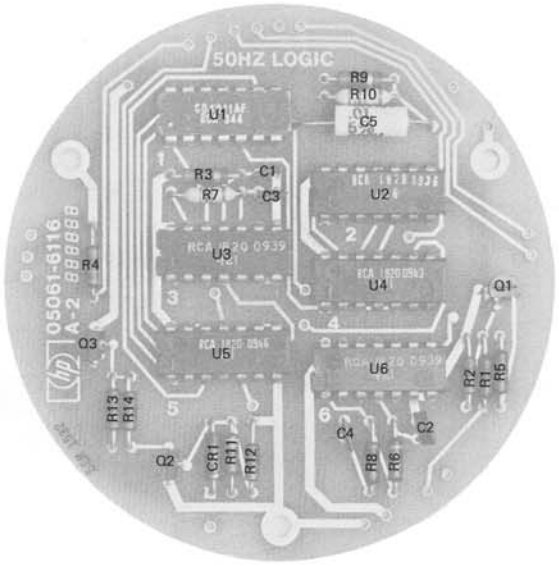
A19 FRONT PANEL (WITH OPTION 003)
(SERIES 1532 OR 1740)



A19 DIGITAL CLOCK



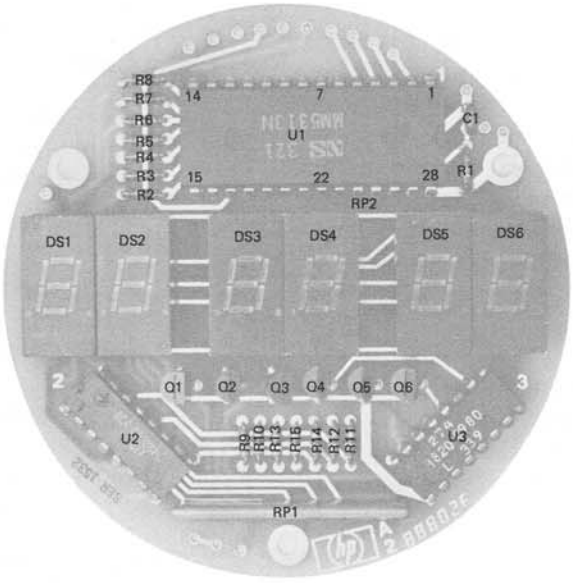
A19A1 5V REGULATOR



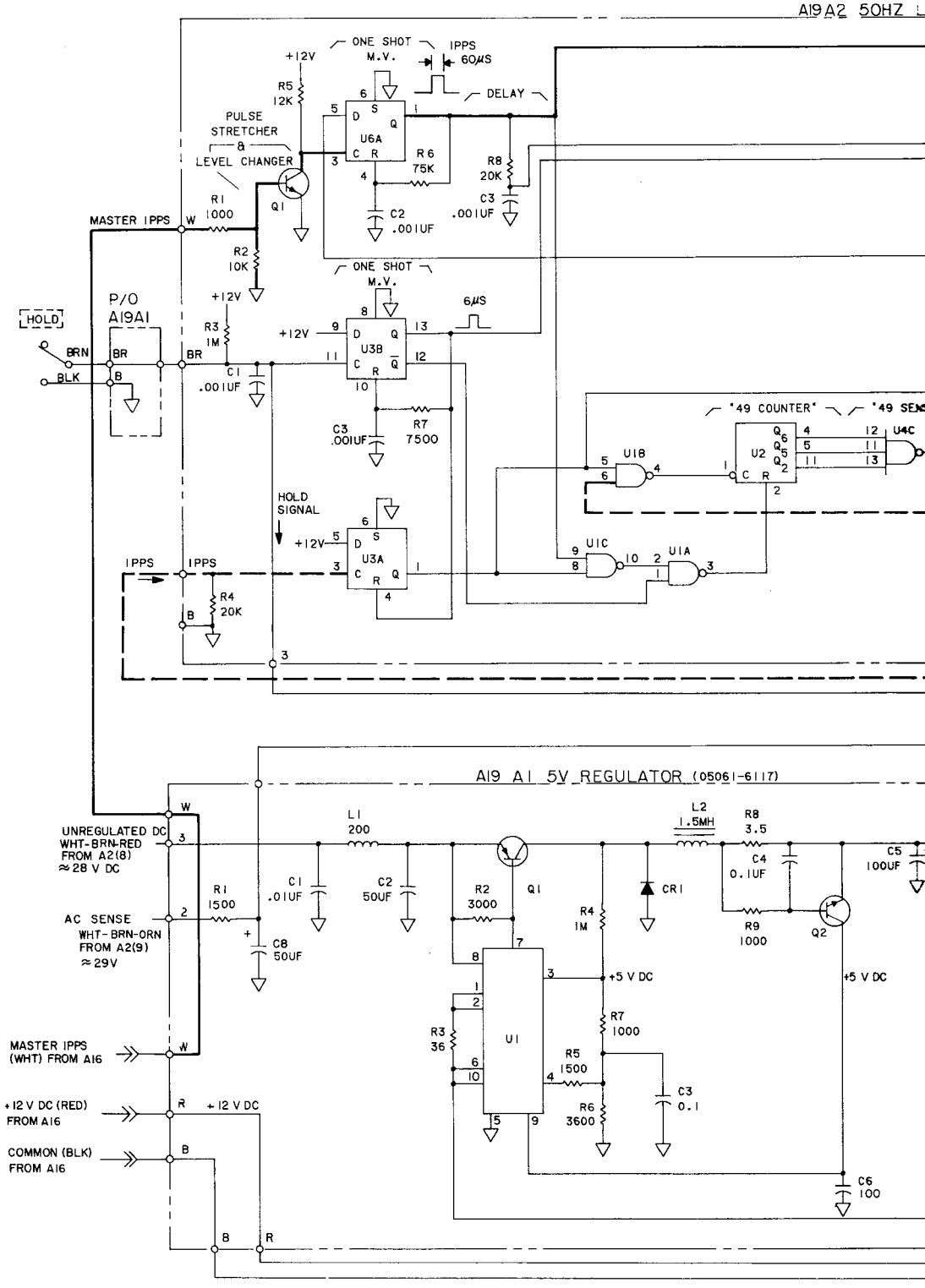
A19A2 50 Hz LOGIC

Figure 7-17
A19 LED DIGITAL CLOCK ASSEMBLY

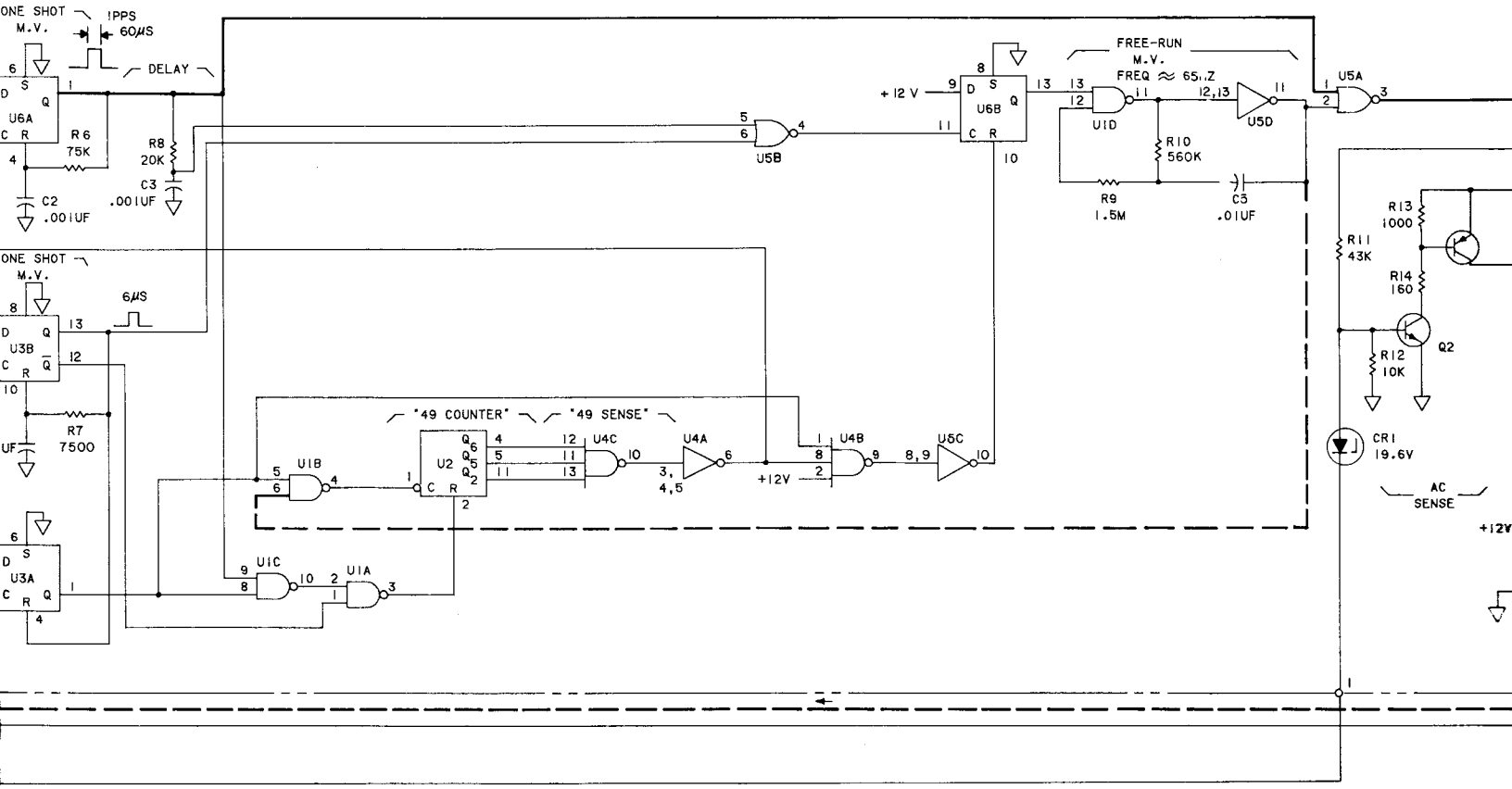
(See Page 7-51)



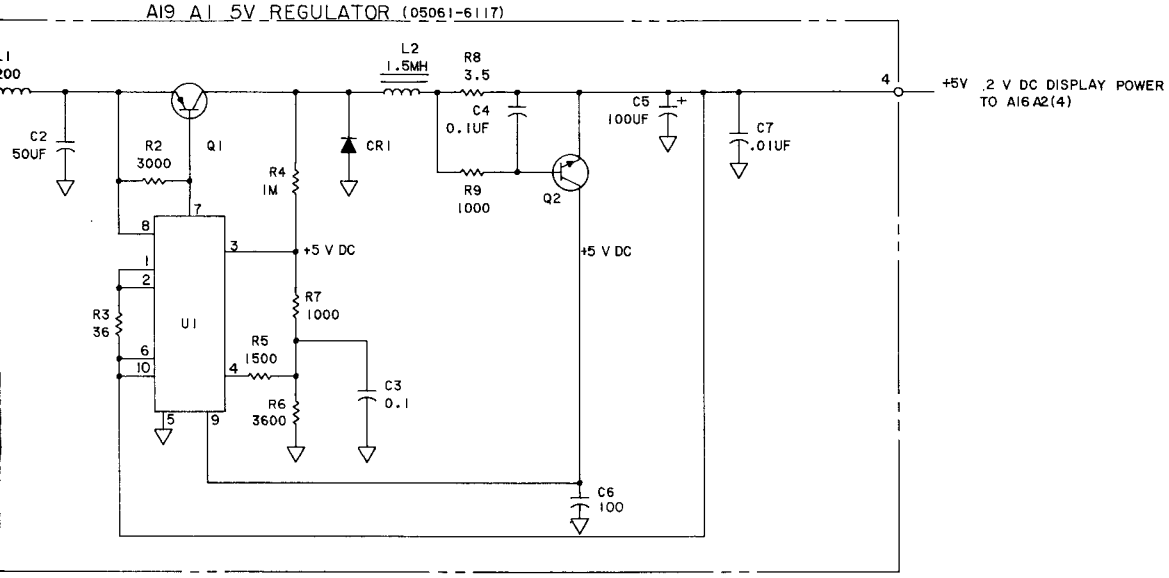
A19A3 CLOCK DISPLAY

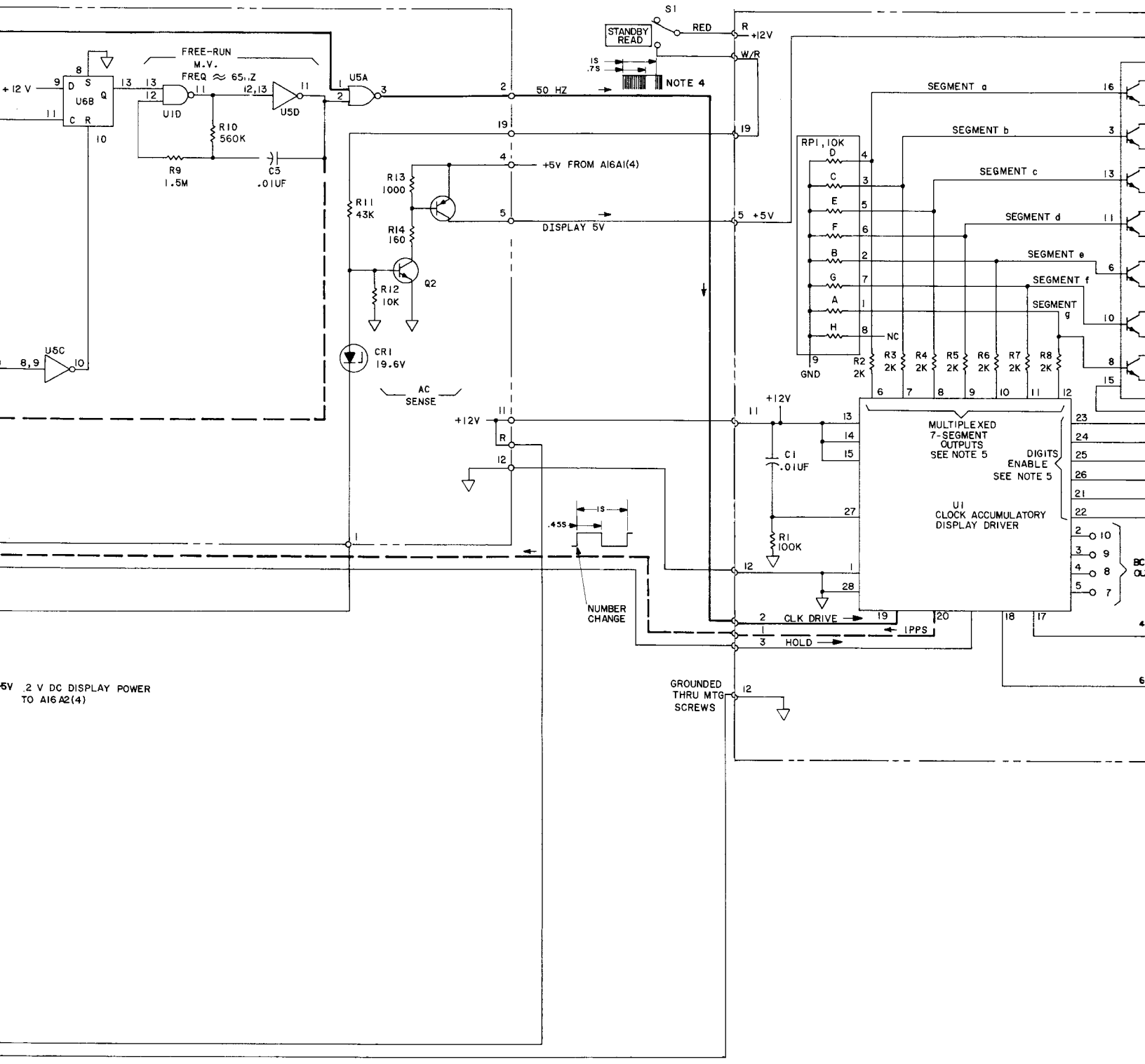

A19A2 50HZ
ONE SHOT M.V.
IPPS 60µS
DELAY
+12V
R5 12K
PULSE STRETCHER & LEVEL CHANGER
Q1
R1 1000
MASTER IPPS
W
R2 10K
U6A
R6 75K
R8 20K
C3 .001UF
C2 .001UF
ONE SHOT M.V.
6µS
P/O A19A1
HOLD
BRN
BLK
BR
B
R3 1M
C1 .001UF
U3B
C3 .001UF
R7 7500
"49 COUNTER"
"49 SENS
U2
U4C
U1B
HOLD SIGNAL
U3A
IPPS
R4 20K
U1C
U1A
A19 A1 5V REGULATOR (05061-6117)
UNREGULATED DC WHT-BRN-RED FROM A2(8) ≈28 V DC
AC SENSE WHT-BRN-ORN FROM A2(9) ≈29V
MASTER IPPS (WHT) FROM A16
+12 V DC (RED) FROM A16
COMMON (BLK) FROM A16
+12 V DC
L1 200
L2 1.5MH
R8 3.5
C4 0.1UF
C5 100UF
C1 .01UF
C2 50UF
R2 3000
Q1
CR1
R1 1500
C8 50UF
R4 1M
R9 1000
Q2
+5 V DC
R7 1000
R3 36
U1
R5 1500
R6 3600
C3 0.1
C6 100

A19A2 50HZ LOGIC (05061-6116)



A19 A1 5V REGULATOR (05061-6117)




S1
STANDBY READ
RED
R
+12V
W/R
.1S
.7S
NOTE 4
FREE-RUN
M.V.
FREQ ≈ 65.2
U6B
U1D
U5D
U5A
R10
560K
R9
1.5M
C3
.01UF
50 HZ
+5V FROM A16A1(4)
R13
1000
R11
43K
R14
160
R12
10K
Q2
DISPLAY 5V
+5V
CR1
19.6V
AC
SENSE
U5C
8,9
10
+12V
RP1, 10K
D
C
E
F
B
G
A
H
NC
GND
R2
2K
R3
2K
R4
2K
R5
2K
R6
2K
R7
2K
R8
2K
SEGMENT a
SEGMENT b
SEGMENT c
SEGMENT d
SEGMENT e
SEGMENT f
SEGMENT g
C1
.01UF
R1
100K
MULTIPLEXED
7-SEGMENT
OUTPUTS
SEE NOTE 5
DIGITS
ENABLE
SEE NOTE 5
U1
CLOCK ACCUMULATORY
DISPLAY DRIVER
.45S
1S
NUMBER
CHANGE
CLK DRIVE
1PPS
HOLD
GROUNDED
THRU MTG
SCREWS
5V .2 V DC DISPLAY POWER
TO A16A2(4)

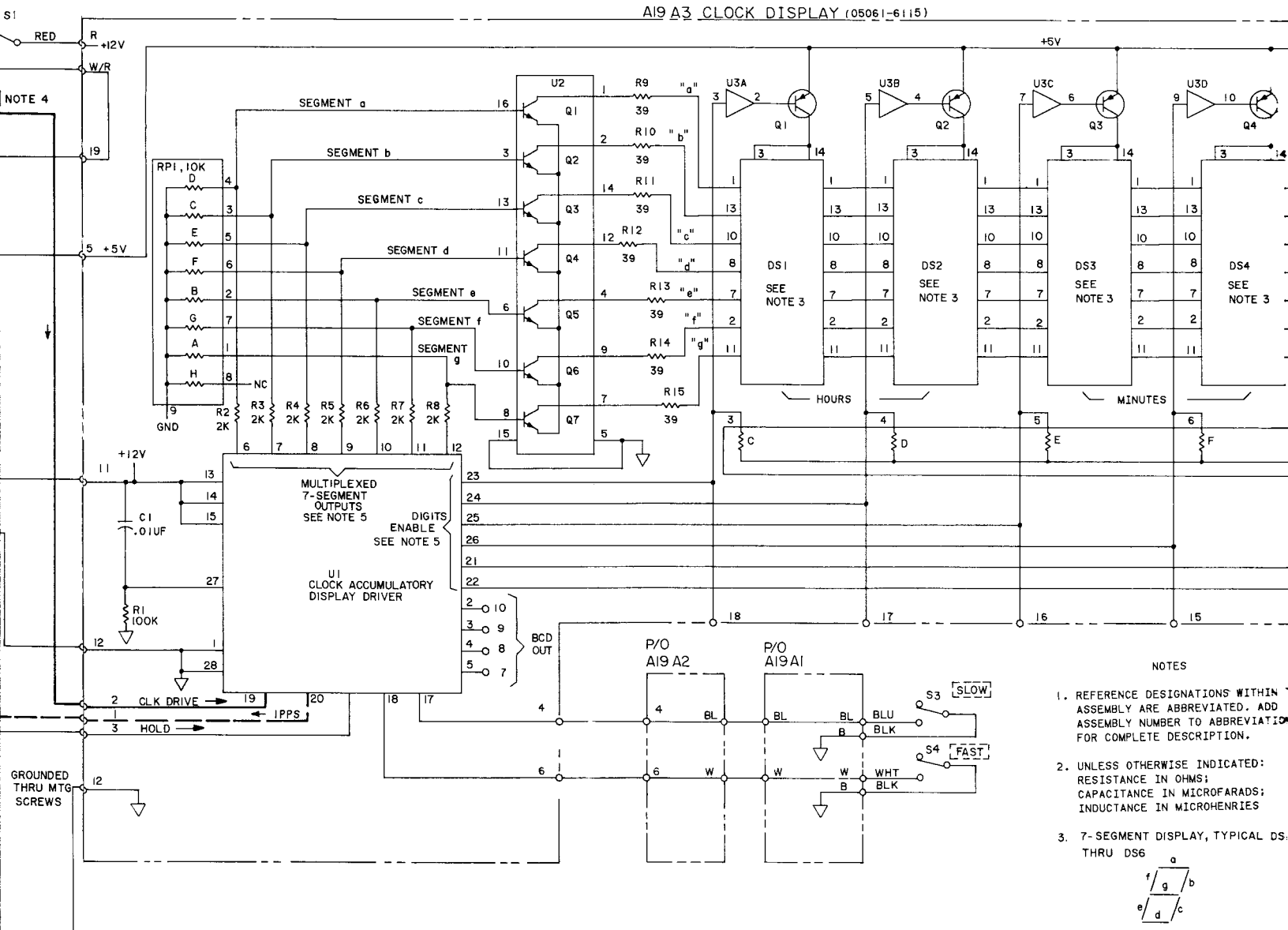
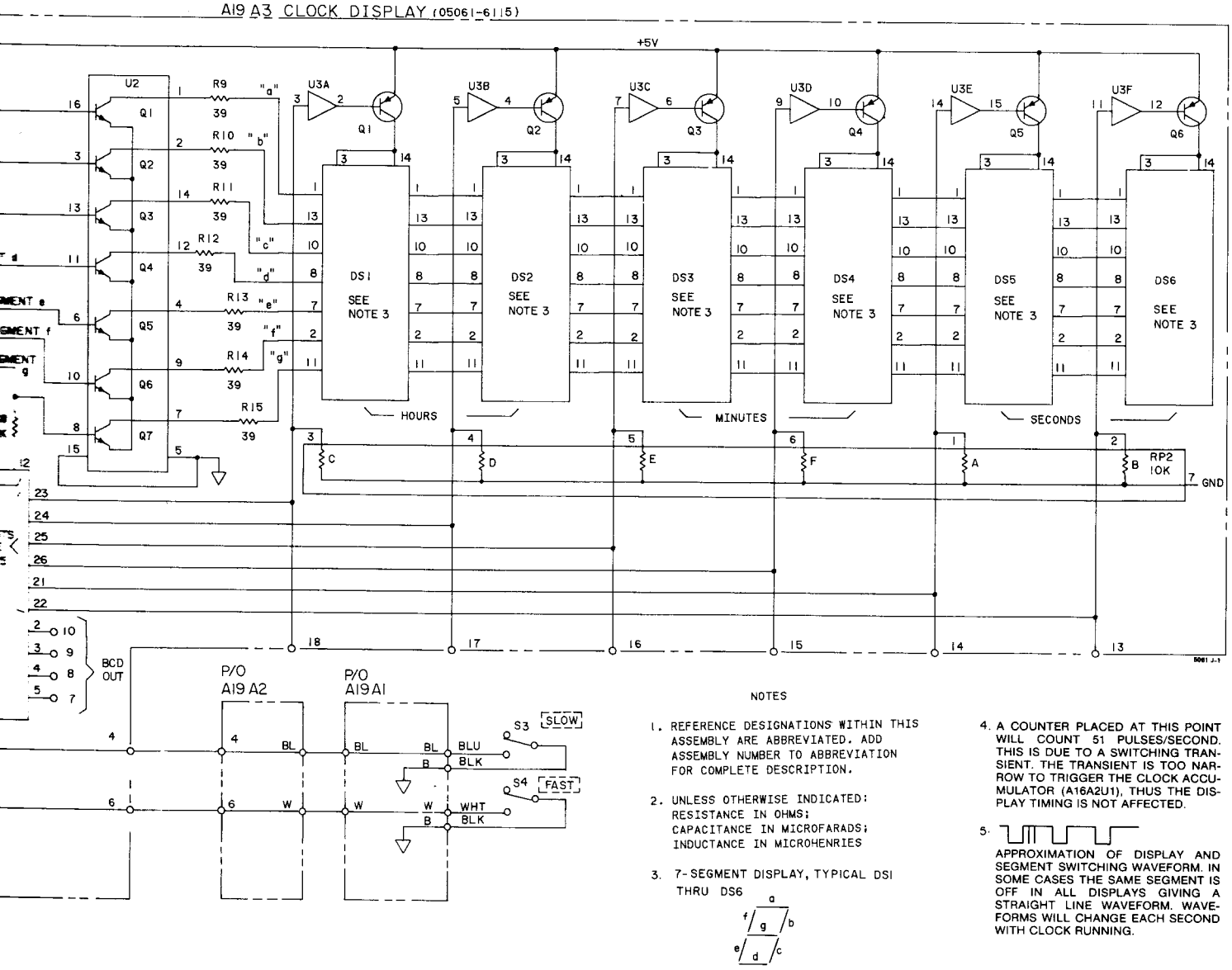

A19 A3 CLOCK DISPLAY (05061-6115)
S1
RED
R
+12V
W/R
NOTE 4
19
5 +5V
+5V
RP1, 10K
D
C
E
F
B
G
A
H
NC
GND
R2 2K
R3 2K
R4 2K
R5 2K
R6 2K
R7 2K
R8 2K
SEGMENT a
SEGMENT b
SEGMENT c
SEGMENT d
SEGMENT e
SEGMENT f
SEGMENT g
U2
Q1
Q2
Q3
Q4
Q5
Q6
Q7
R9 "a" 39
R10 "b" 39
R11 39
R12 "c" 39
R13 "e" 39
"d"
"f"
R14 "g" 39
R15 39
U3A
U3B
U3C
U3D
DS1 SEE NOTE 3
DS2 SEE NOTE 3
DS3 SEE NOTE 3
DS4 SEE NOTE 3
HOURS
MINUTES
+12V
C1 .01UF
R1 100K
MULTIPLEXED 7-SEGMENT OUTPUTS SEE NOTE 5
DIGITS ENABLE SEE NOTE 5
U1 CLOCK ACCUMULATORY DISPLAY DRIVER
BCD OUT
CLK DRIVE
1PPS
HOLD
GROUNDED THRU MTG SCREWS
P/O A19 A2
P/O A19 A1
S3 SLOW
S4 FAST
BLU
BLK
WHT
BLK
NOTES
1. REFERENCE DESIGNATIONS WITHIN ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATIO FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN MICROFARADS; INDUCTANCE IN MICROHENRIES
3. 7-SEGMENT DISPLAY, TYPICAL DS THRU DS6

Figure 7-1



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN MICROFARADS; INDUCTANCE IN MICROHENRIES

3. 7-SEGMENT DISPLAY, TYPICAL DS1 THRU DS6

4. A COUNTER PLACED AT THIS POINT WILL COUNT 51 PULSES/SECOND. THIS IS DUE TO A SWITCHING TRANSIENT. THE TRANSIENT IS TOO NARROW TO TRIGGER THE CLOCK ACCUMULATOR (A16A2U1), THUS THE DISPLAY TIMING IS NOT AFFECTED.

5.

APPROXIMATION OF DISPLAY AND SEGMENT SWITCHING WAVEFORM. IN SOME CASES THE SAME SEGMENT IS OFF IN ALL DISPLAYS GIVING A STRAIGHT LINE WAVEFORM. WAVEFORMS WILL CHANGE EACH SECOND WITH CLOCK RUNNING.

Figure 7-17. A19 LED Digital Clock Assembly

CHANGE 20 (1532A00631 and below):

Under Change 19 (this section) A19 Parts List and schematic diagram delete A2C6. Ignore all reference to a third A19 board acting as a shield.

CHANGE 21 (1532A632 through 1532A790):

Page 1-4, Table 1-3:
Change CLOCK MOVEMENT to read "24 hour mechanical clock."

Page 3-9, Paragraph 3-21:
Replace with the following:

"The TIME STANDARD OPTION includes a mechanical clock movement indicating time in hours, minutes, and seconds. FAST and STOP pushbuttons on the divider module (Figure 3-10) permit setting the clock movement to the nearest second. The hour and minute adjustment is the knob located on the back of the clock movement. To set, remove the top cover; then reach in and pull out the knob to engage and set the clock. Push this knob back in to release. The SYNC pushbutton allows the 5065A to be synchronized to an external clock pulse.

Page 3-9, paragraph 3-25(f):
Replace paragraph with:

When the clock pulse is synchronized, the mechanical clock in the 5065A will run in step. The set knob at the rear of the clock provides coarse adjustment of hours and minutes. The FAST and STOP switches on the A5 module provide a way to speed up or stop the clock for adjustment to the nearest second."

Page 3-9, paragraph 3-28:
Replace with: "Setting the Mechanical Clock".

a. Remove top cover for access. Use the set knob at the rear of the clock; pull out to engage and set.

b. The FAST and STOP pushbuttons on A5 are accessible with the top cover removed 10 PPS is routed to the clock with the FAST pushbutton depressed. The STOP pushbutton disconnects the clock drive.

Page 3-15, Figure 3-11:
Add attached TOP OPERATING CONTROLS Figure 7-18.

Page 4-2, paragraph 4-17:
Replace paragraph with the following:

Additional A5 controls are the FAST, STOP, and SYNC switches. The FAST pushbutton speeds up the clock movement by replacing the 1 PPS clock drive with 10 PPS. The STOP pushbutton shorts the 1 PPS clock drive to ground to stop the clock.

To synchronize the 1 PPS with an external reference pulse, the SYNC pushbutton is depressed for 1 second then released. If a sync pulse is connected to the rear SYNC INPUT jack, one reference pulse will enter the synchronizing circuits during the 1 second interval. This pulse will reset the digital divider. The output 1 PPS "tick" pulse from the 1 PPS front panel jack will then be in "sync" with the reference pulse.

Page 6-2, Figure 6-1 item 4:
Change Panel: Left insert; to 05065-0011. Door Panel; to 05065-0015. Standard Panel Insert; to 05065-00122. Panel Option 002 Insert; to 05065-0014.

Page 6-26, Table 6-5:
Added A5B1, 05065-6085.
Change 05065-0048, Chassis: Digital Divider to 05065-0037.
Change A5,05065-6084, Module Assy Digital Divider to 05065-6025. Add A5S1 3101-0052; SWITCH: PUSHBUTTON SPST; 82389; 961 LESS HWD and A5S3 Same as A5S1.

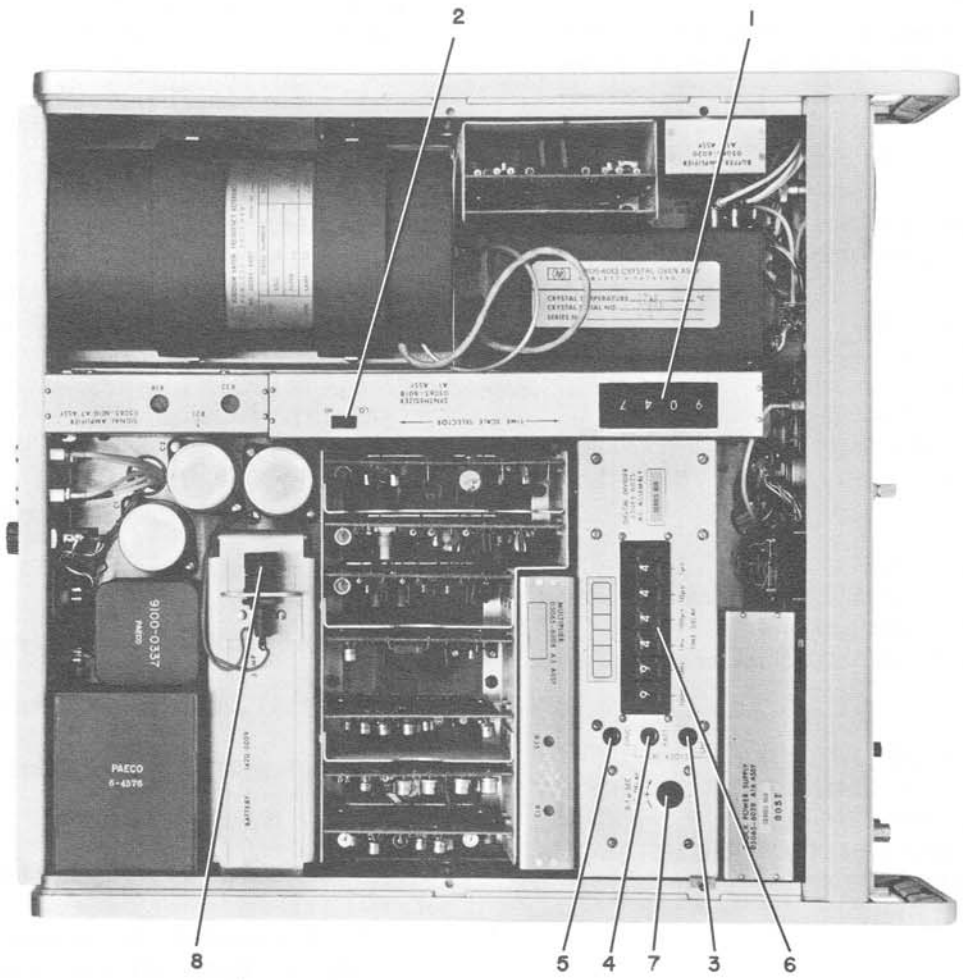
Page 6-27, Table 6-5:
Change A16 from 05065-6085 to 05065-6028.
Change A16A1 from 05065-6082 to 05065-6029.
Add: A16IC1 1820-0313 IC; DTL RS/JK CLOCKED F/F; 28480; 1820-0313
A16A1Q11 and Q12; 1854-0020; TSTR;SI NPN; 28480; 1854-0020.
A16A1CR13 and CR14; 1902-0554; DIODE BREAKDOWN: 10V 1W; 28480; 1902-0554

Page 6-30, Table 6-5:
Add Table 7-11 resistor parts list to A16 (R21 to R26).

Table 7-11. A16 Resistor Parts List

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Part Number
A16A1R21	0757-0931	2	R: FXD FLM 2K OHM 2% 1/8W	28480	0757-0931
A16A1R22	0757-0931		R: FXD FLM 2K OHM 2% 1/8W	28480	0757-0931
A16A1R23	0757-0924	2	R: FXD MET FLM 1K OHM 2% 1/8W	28480	0757-0924
A16A1R24	0757-0924		R: FXD MET FLM 1K OHM 2% 1/8W	28480	0757-0924
A16A1R25	0757-0920		R: FXD FLM 680 OHM 2% 1/8W	28480	0757-0920
A16A1R26	0757-0920		R: FXD FLM 680 OHM 2% 1/8W	28480	0757-0920

Figure 7-18. Top Operating Controls



1. Synthesizer TIME CLOCK SELECTOR thumbwheel switch: selects synthesized frequency.

2. Synthesizer TIME SCALE SELECTOR HI-LO switch: used with thumbwheel switch to select synthesized frequency.

3. CLOCK SET STOP switch (Option 001 only). digital clock is stopped when switch is depressed, starts when released.

4. CLOCK SET FAST switch (Option 001 only): digital clock second hand is accelerated when switch is depressed, resumes normal operation when released.

5. Clock SYNC switch (Option 001 only): Synchronizes digital clock with an external clock when depressed; clock remains synchronized when released.

6. Clock TIME DELAY thumbwheel switch (Option 001 only): selects time delay between an external reference pulse and the internal 1 pulse-per-second clock pulse. Adjustable in decade steps from 1 μs to 1 sec.

7. 0-1 μSEC TIME DELAY control (Option 001 only): Allows continuous adjustment of clock pulse delay over any 1 μsec range.

8. Battery fuse: removed momentarily to disconnect optional standby battery from circuit for storage or shipment. Battery will remain disconnected after fuse is replaced.

Page 8-33, Figure 8-133:
Change A5, Digital Divider Assy to 05065-6025
Add A5S1 and S3 switches to schematic as shown in Figure 7-19.

See Figure 8-13 of old manual

Page 8-35, Figure 8-14 and Page 8-37, Figure 8-15:
Change A5 Digital Divider Assy to 05065-6025.

Page 8-73, Figure 8-28:
Change A16, Digital Divider Power Supply Assy to 05065-6028.
Change A16A1 to 05065-6029.
Replace schematic diagram with A16A1 schematic diagram shown in Figure 7-20.

Page 8-69, Figure 8-26:
Add resistor A14R15 between the cathode of A14CR2 and ground (value of 5100 ohms).
Change A14R12 to 1000 ohms and A14R16 to 150k ohms.

Page 6-16, Table 6-2:
Add A14R15; 0757-0941; R:FXD 5.1k OHMS 2% 1/8 W; 28480; 0757-0941.
Change A14R12 to 0757-0924; R:FXD MET 1k OHM 2% 1/8 W; 28480; 0757-924.
Change A14R16 to 0757-0976; R:FXD FLM 150k OHM 2% 1/8W; 28480; 0757-0976.

Page 6-3 and 6-4, Table 6-2, A1 (15065-6076) Replaceable Parts:
Change A1A1R3 to 0698-3617; R:FXD MET FLM 100 OHM 2% 1/8W; 28480; 0698-3617.

Page 8-17 and 8-19, Figure 8-9, A1 Schematic Diagrams:
Change A1A1R3 to 51 OHMS.

CHANGE 22 (1736):

Page 6-18, Table 6-2, Replaceable Parts:
Change fuseholders F1 and F2 part numbers (three pieces each) to 1400-0085 for both fuseholders.

CHANGE 23 (1820):

Page 6-16, Table 6-2, A15 (05065-6023) Replaceable Parts:
Add "(SERIES PREFIX 1820)" to A15 "Description".
Change A15R17 from 2100-1774 to 2100-1773 in "HP" and "Mfr" part number columns. The 2100-1773 control has a value of 1000 ohms.

Page 8-71, Figure 8-27, A15 Schematic Diagram:
Change A15 series number from 1840 (not shown on schematic) to "SERIES 1416".

Change value of A15R17 from 2000 ohms to 1000 ohms.

CHANGE 24 (1840):

Page 6-3 and 6-4, Table 6-2, Replaceable Parts:
Change A1 Module 05065-6076 series number from 1908 to 1736.
Change A1A1Q20 from 1854-0547 to 1854-0035; TRANSISTOR NPN SI; 28480; 1854-0035.
Page 8-17, Figure 8-9, Sheet 1 of 2 Schematic Diagram:
Change A1 and A1A1 series number from 1908 to 1736.
Page 8-19, Figure 8-9, Sheet 2 of 2 Schematic Diagram:
Change A1 and A1A1 series number from 1908 to 1736.
Change A1A1Q20 from 2N3725 to 1854-0035.

CHANGE A (Option 001 A16 Series 1532 only)

NOTE

The following change for A16 series number does not affect the serial prefix number of the instrument in which A16 is installed. Module assembly A16 is added only when Option 001 or 003 is added. Consequently, the series for A16 may not be the same as the instrument serial prefix number.

Page 6-27, Table 6-5, Option 001 to 003 Replaceable Parts:
Change A16 and A16A1 from series 1912 to 1532.
Change A16A1Q8 from 1854-0547 to 1854-0035, TRANSISTOR NPN SI TO-5; 28480; 1854-0035
Page 8-73, Figure 8-28, A16 Schematic Diagram:
Change A16 and A16A1 series number from 1912 to 1532.
Change A16A1Q8 from 2N3725 to 1854-0035.

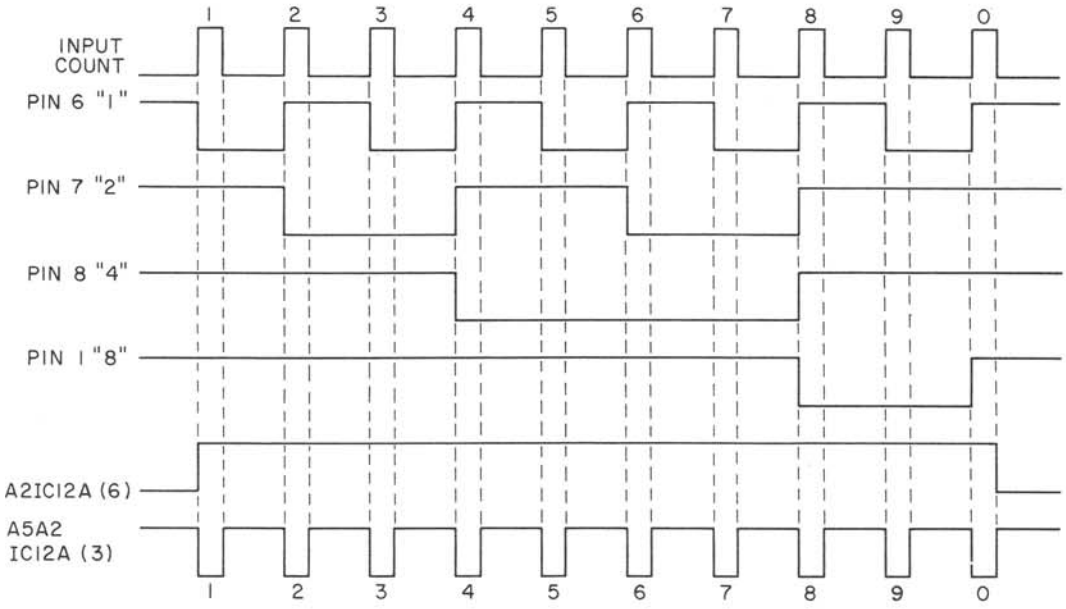
CHANGE B (Option 001 A5 Series 1840 only)

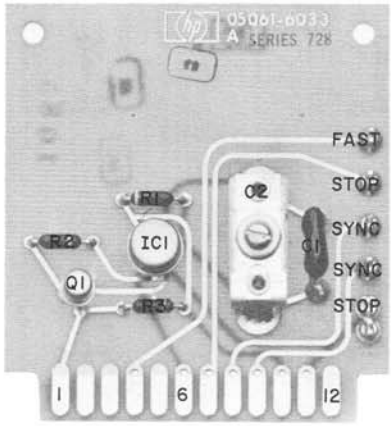
NOTE

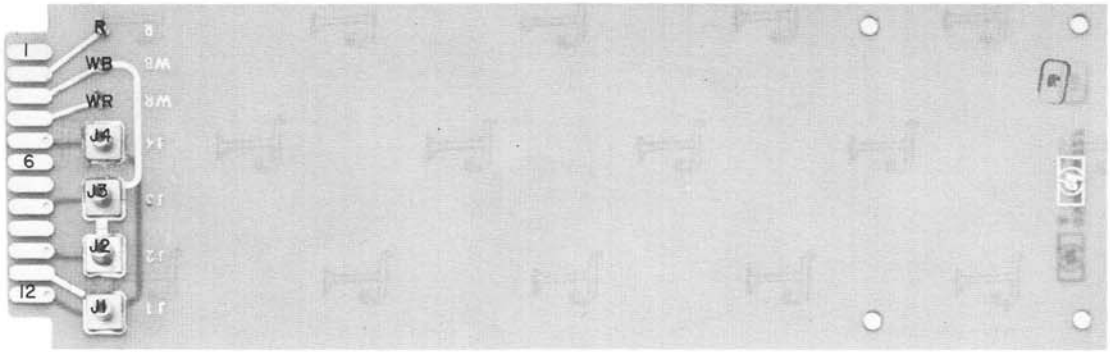
The following changes for A5 series number does not affect the serial prefix number of the instruments with A5 added for Option 001 or 003. The series number of the A5 module assembly may not be the same as the instrument serial prefix number.

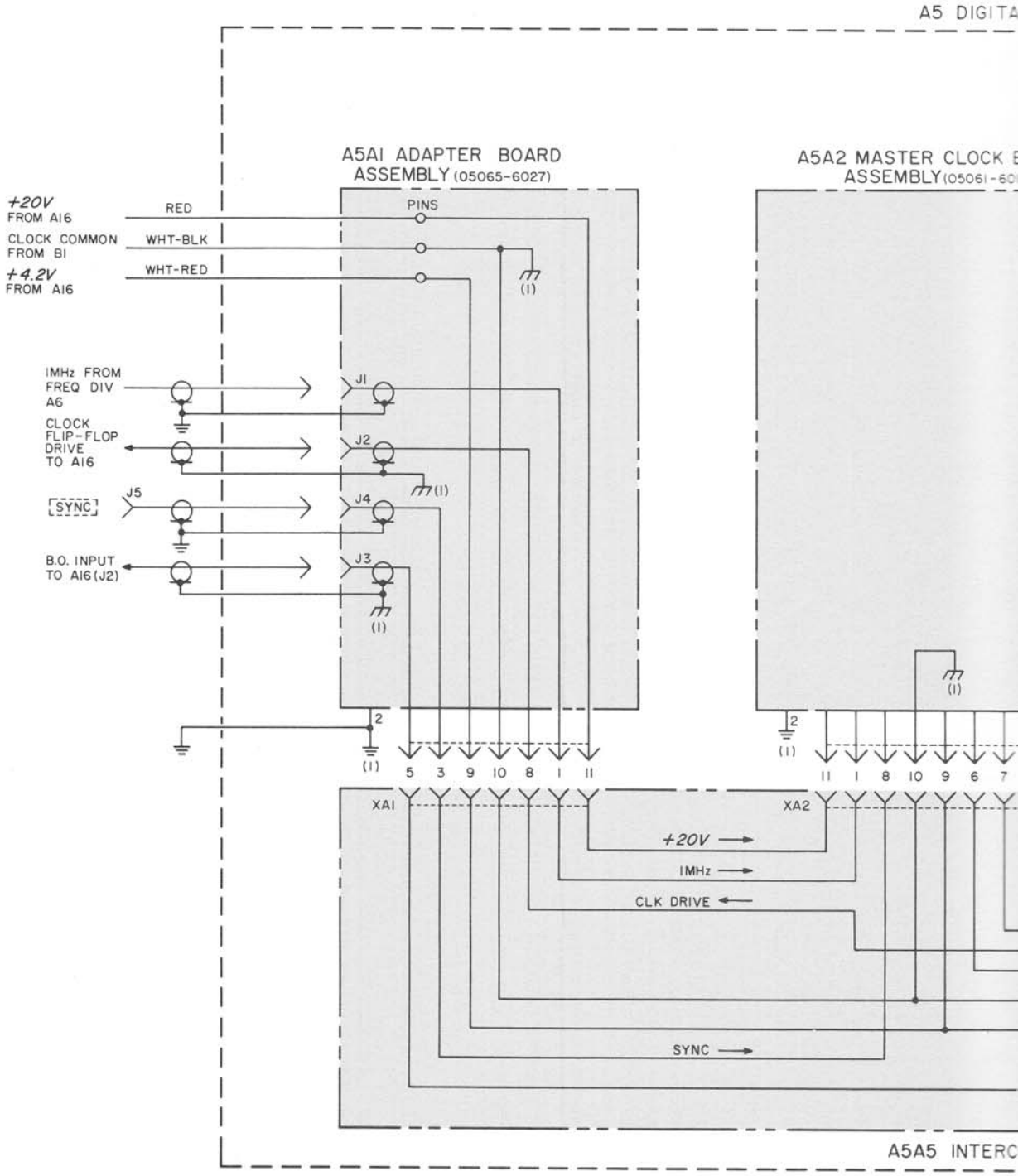
Figure 7-19
A5 DIGITAL DIVIDER ASSEMBLY

(See Page 7-55)


1 2 3 4 5 6 7 8 9 0
INPUT COUNT
PIN 6 "1"
PIN 7 "2"
PIN 8 "4"
PIN 1 "8"
A2IC12A (6)
A5A2 IC12A (3)
1 2 3 4 5 6 7 8 9 0

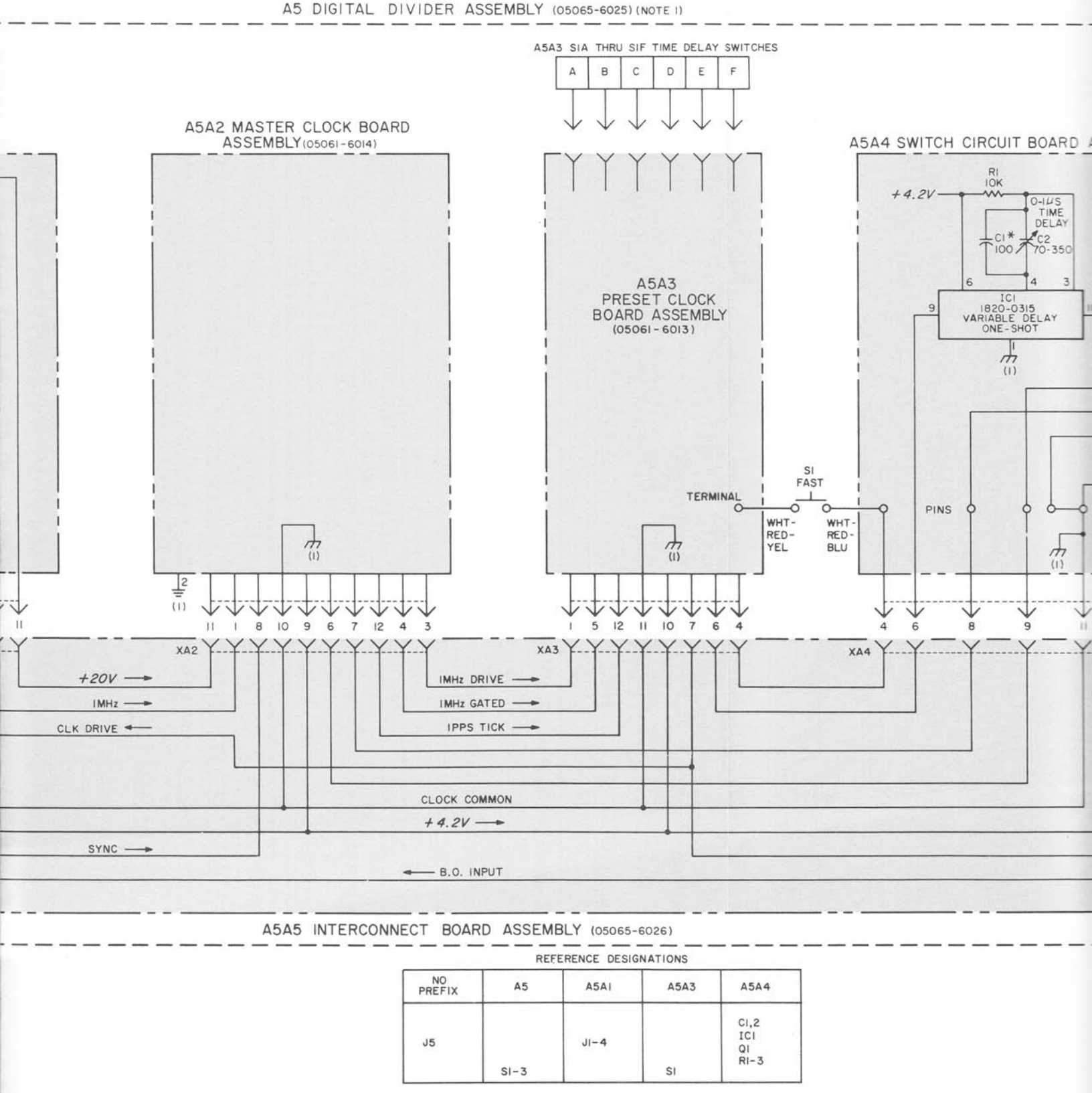

05061-6033
A SERIES 728
FAST
STOP
SYNC
SYNC
STOP
R1
R2
R3
IC1
Q1
Q2
C1
1
6
12


R
WB
WR
1
6
12
J4
J3
J2
J1



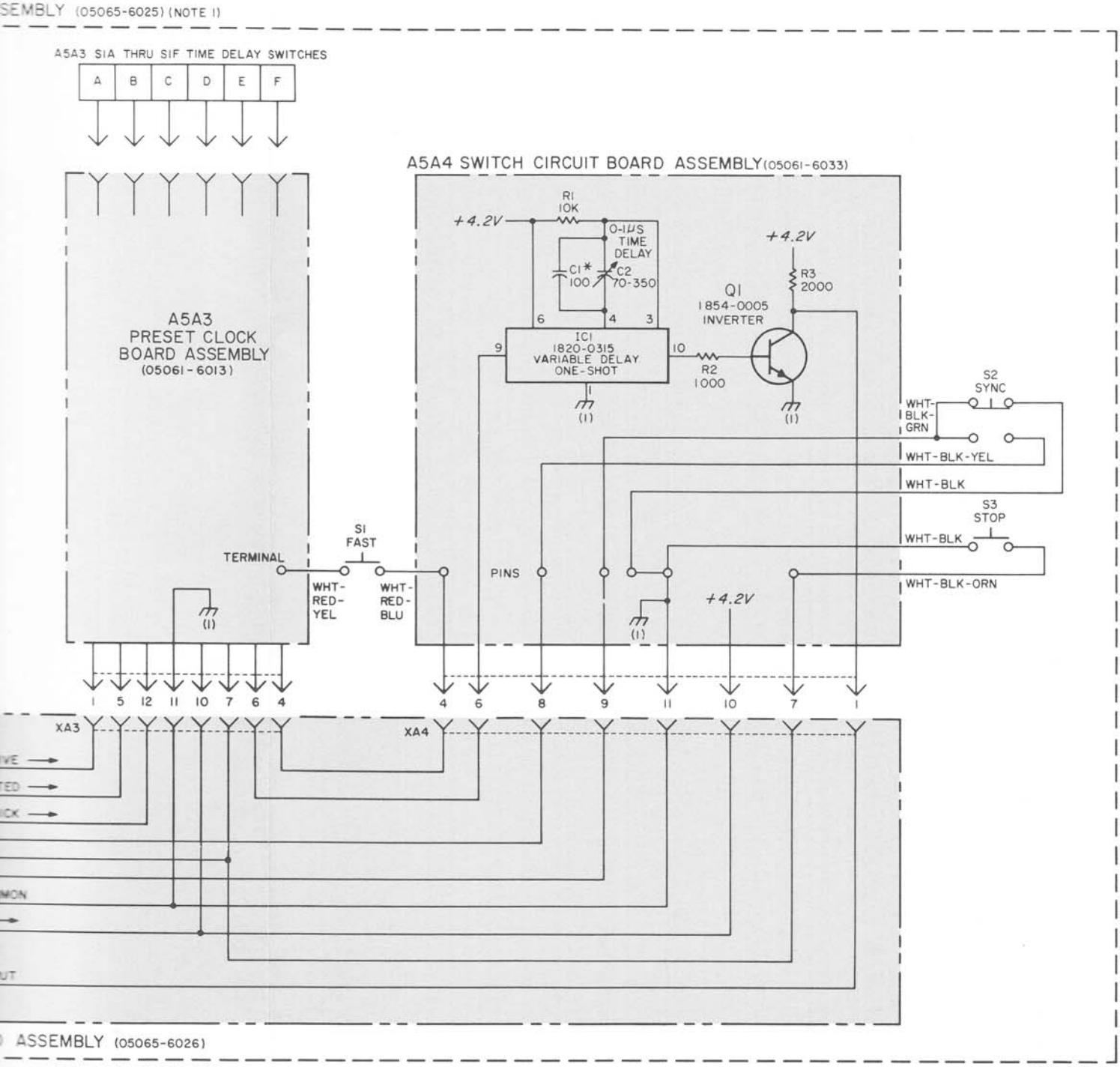
NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN.



REFERENCE DESIGNATIONS

NO PREFIX	A5	A5A1	A5A3	A5A4
J5	SI-3	J1-4	SI	C1,2 IC1 Q1 R1-3



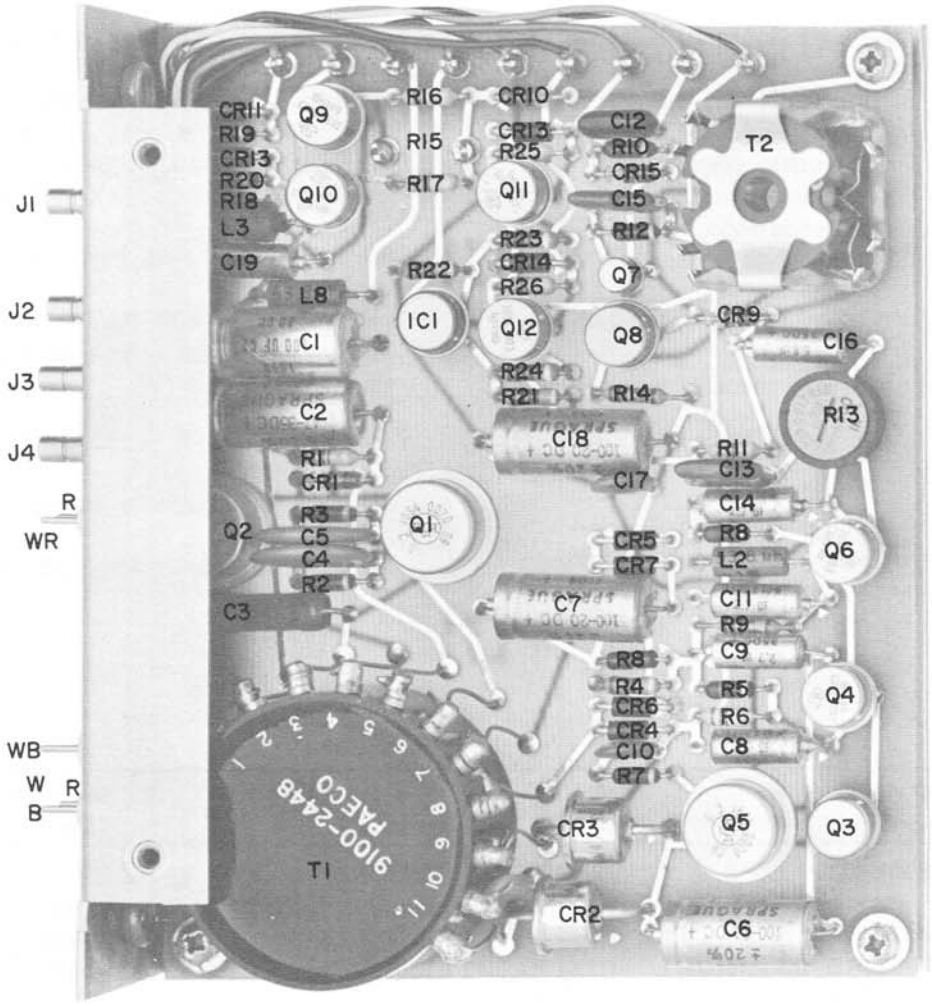
REFERENCE DESIGNATIONS

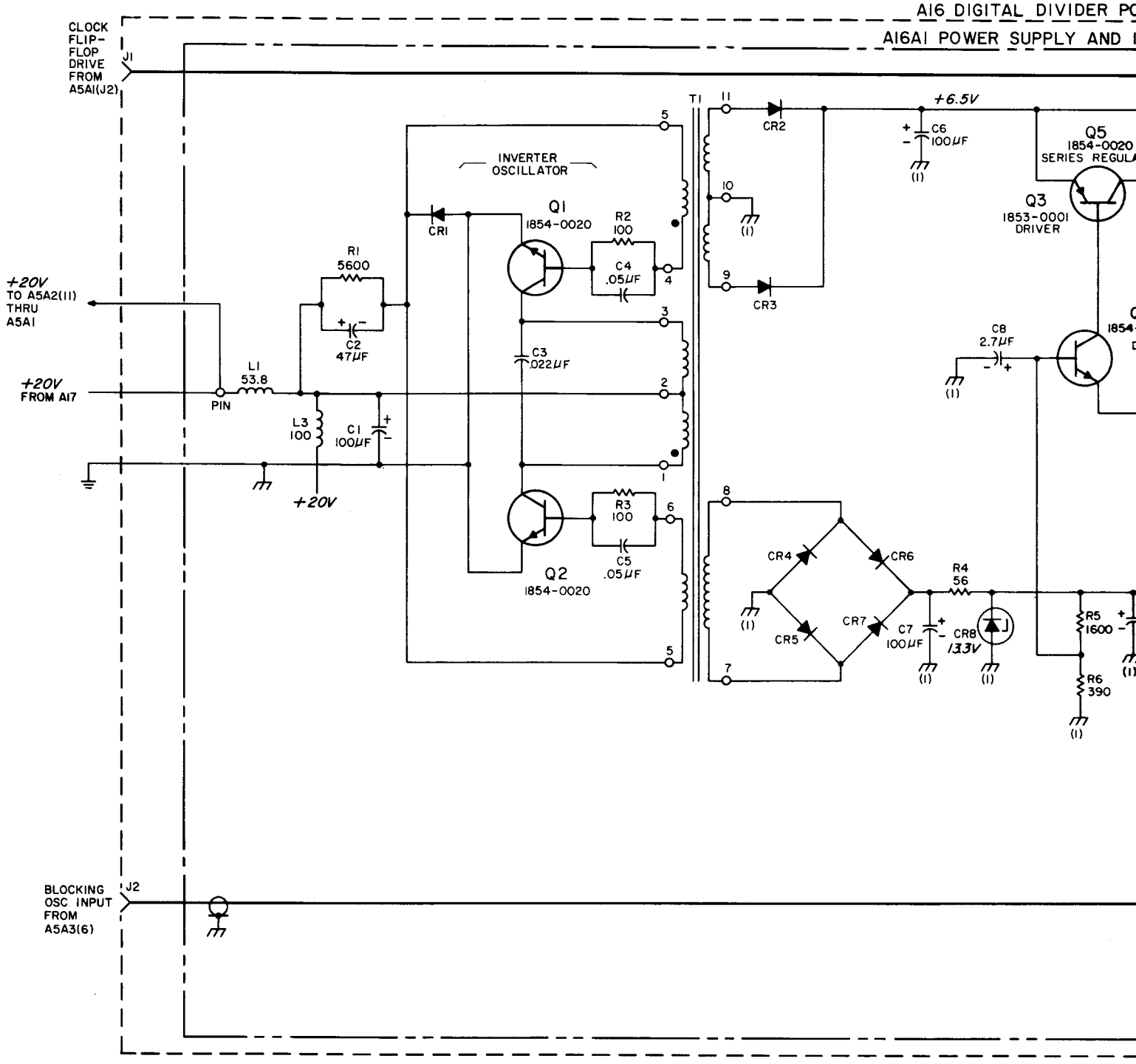
A5	A5A1	A5A3	A5A4
S1-3	J1-4	S1	C1,2 IC1 Q1 R1-3

Figure 7-19. A5 Digital Divider Assembly

Figure 7-20
A16 DIGITAL DIVIDER POWER SUPPLY ASSEMBLY

(See Page 7-57)


CR11
RI9
CR13
R20
RI8
L3
C19
J1
J2
J3
J4
R
WR
WB
W
R
B
Q9
Q10
RI6
RI5
RI7
CR10
CR13
R25
Q11
R23
CR14
R26
Q7
R22
IC1
Q12
Q8
R24
R21
RI4
C18
C17
CR5
CR7
C7
R8
R4
CR6
CR4
C10
R7
CR3
CR2
Q5
C6
C12
RI0
CR15
C15
RI2
T2
CR9
C16
RI3
RI1
C13
C14
R8
L2
C11
R9
C9
R5
R6
C8
Q6
Q4
Q3
L8
C1
C2
RI
CR1
R3
C5
C4
R2
C3
Q2
Q1
T1
9100-2448
PAECO



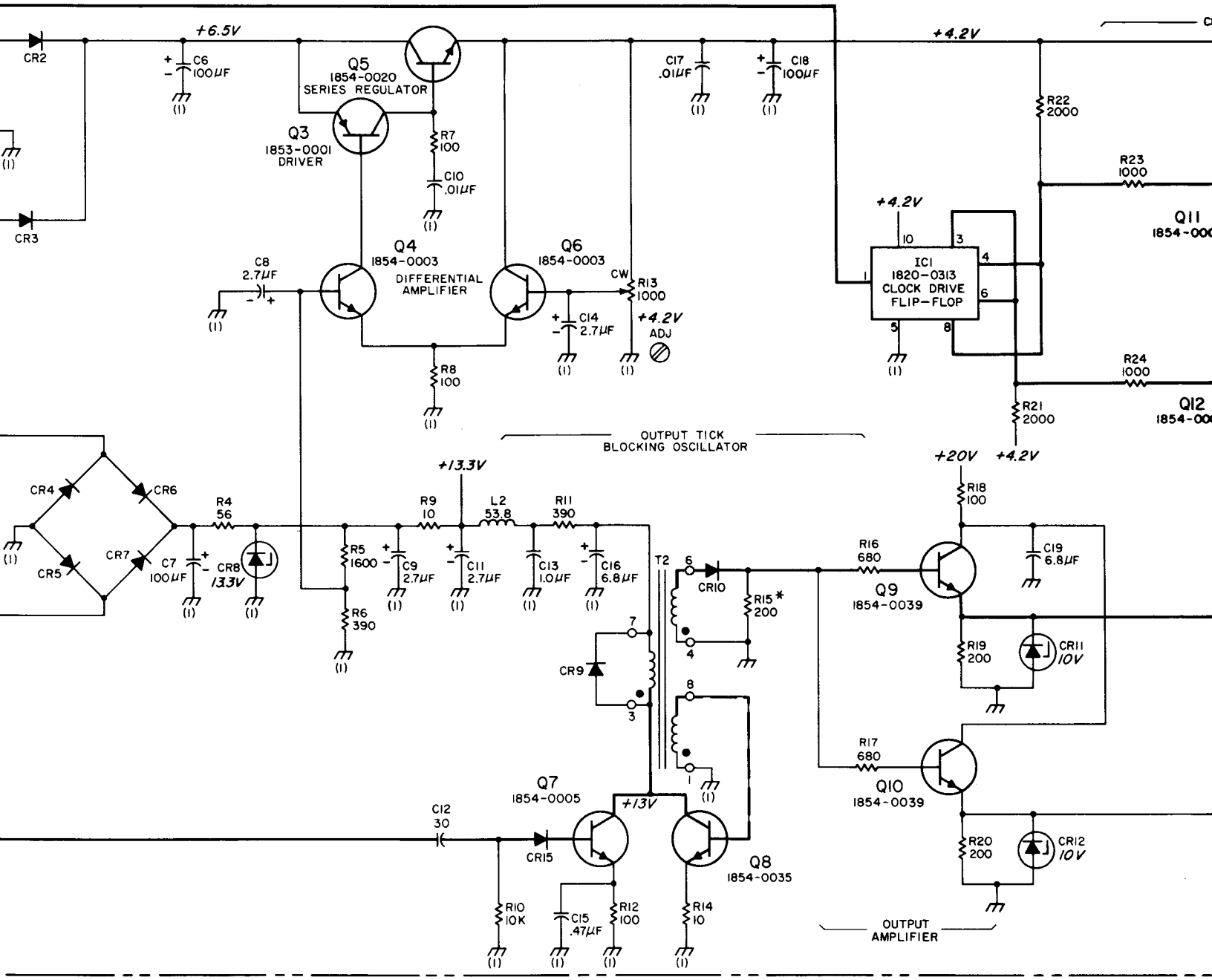
NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS; INDUCTANCE IN MICROHENRIES
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN

NO PREFIX
J14

A16 DIGITAL DIVIDER POWER SUPPLY ASSEMBLY (05065-6028) (NOTE 1) SERIES 1104

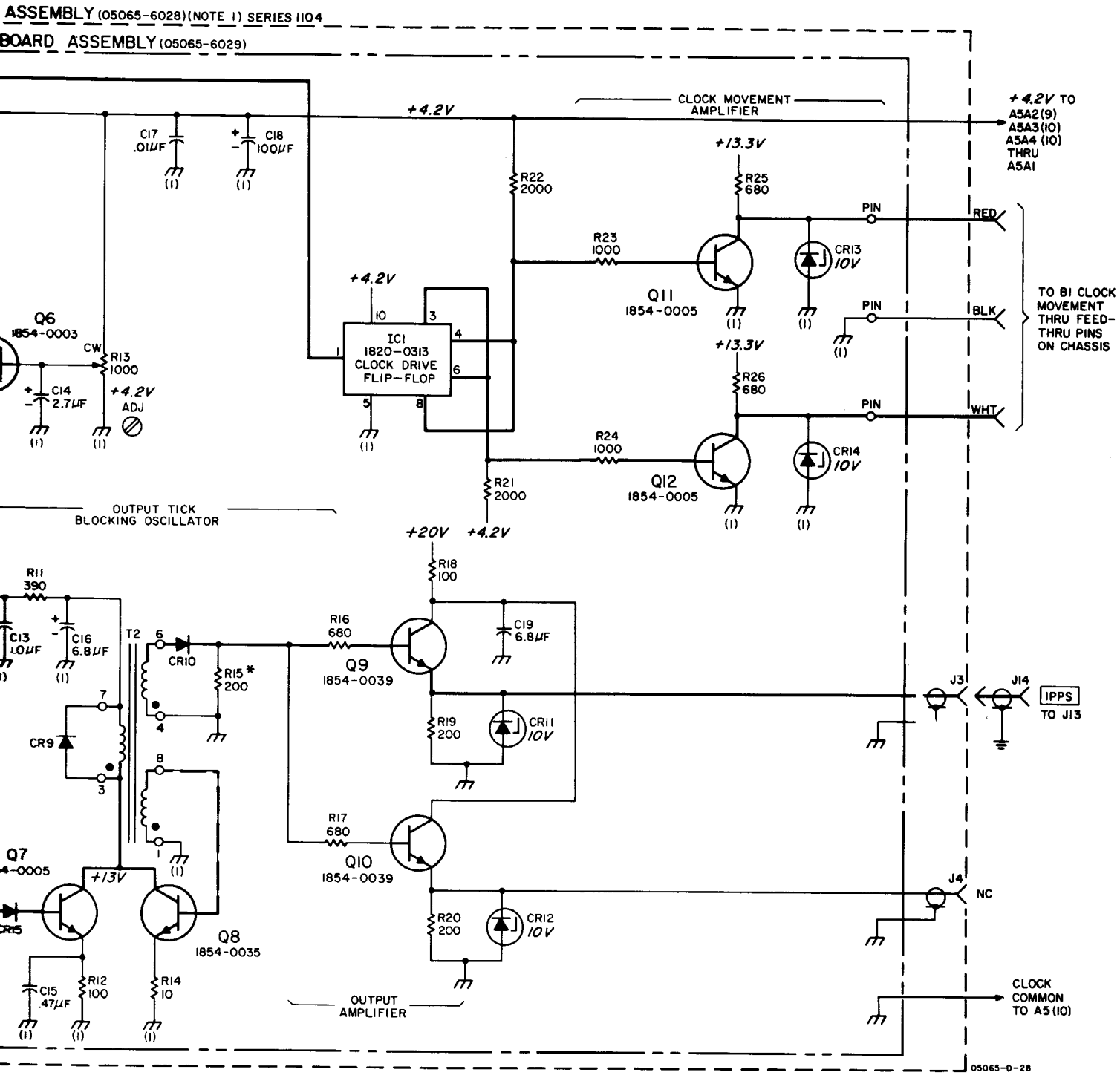
A16A1 POWER SUPPLY AND IPPS OUTPUT BOARD ASSEMBLY (05065-6029)



REFERENCE DESIGNATIONS

NO PREFIX	A16	A16A1
J14	J1-4	C1-19 CR1-15 IC1 L1-3 Q1-12 R1-26 T1,2

Figure



A16A1
C1-19
CR1-15
IC1
L1-3
Q1-12
R1-26
T1,2

Figure 7-20. A16 Digital Divider Power Supply Assembly

Page 6-23, Table 6-4, Option 001 (A5) Replaceable Parts:

Change A5 (05065-6084) series number from 1904 to 1840.

Page 6-26, Table 6-4, Option 001 (A5A4) Replaceable Parts:

Replace A5A4 (05061-6152) and all components for this assembly with A5A4 Part No. 05061-6033 and components in Table 7-12.

A5A4 05061-6033 (1840) PL here

Page 8-33, Figure 8-13, A5 Schematic Diagram:

Change A5 from series 1904 to 1840.

Replace A5A4 schematic diagram with diagram in attached Figure B for A5A4 P.N. 05061-6033 (SERIES 1840) circuit board assembly.

Replace A5A4 component locator illustration with new illustration in attached Figure C.

Page 8-35, Figure 8-14, Part of A5 Schematic Diagram and

Page 8-37, Figure 8-15, Part of A5 Schematic Diagram:

Change A5 series number at top of diagram from series 1904 to 1840.

NOTE

The previous A5A4 circuit board assembly used a variable capacitor instead of the newer potentiometer. The adjustment procedure is the same for both assemblies.

CHANGE C (Option 001 A5 Series 723)

NOTE

The following changes for A5 series number does not affect the serial prefix number of the instruments with A5 added for Option 001 or 003. The series number of the A5 module assembly may not be the same as the instrument serial prefix number.

Page 6-26 and 6-27, Table 6-4, Option 001 to 003 Replaceable Parts:

Change A5 module assembly (05065-6084) and A5A2 (05061-6014) series numbers to SERIES 723.

Change A5A2C13 to 0140-0202 (15 pf); FXD MICA 15PF 5% 500WVDC; 28480; 0140-0202.

Page 8-35, Figure 8-14, Part of A5 Schematic Diagram and

Page 8-37, Figure 8-15, Part of Schematic Diagram:

Change A5 series number at top of both schematics to SERIES 723.

Page 8-35, Figure 8-14, A5A2 (05061-6014) Schematic Diagram:

Change series number at top of schematic to SERIES 723.

Change the value of A5A2C13 from 10pf to 15pf.

Table 7-12. A5A4 Parts List

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Part Number
A5A4	05061-6033	1	BOARD ASSY: SWITCH	28480	05061-6033
A5A4C1	0140-0176	1	C: FXD MICA 100 PF 2%	28480	0140-0176
A5A4C2	0131-0006	1	C: VAR MICA 70-350 PF 175VDCW	28480	0131-0006
A5A4IC1	1820-0315		INTEGRATED CIRCUIT	28480	1820-0315
A5A4Q1	1854-0005		TSTR: SI NPN	80131	2N708
A5A4R1	0757-0948		R: FXD FLM 10K OHM 2% 1/8W	28480	0757-0948
A5A4R2	0757-0924		R: FXD MET FLM 1K OHM 2% 1/8W	28480	0757-0924
A5A4R3	0757-0931		R: FXD FLM 2K OHM 2% 1/8W	28480	0757-0931

SECTION VIII
CIRCUIT DIAGRAMS, THEORY, AND MAINTENANCE

8-1. GENERAL

8-2. This section contains block, wiring, schematic, waveform, and component locators for the Model 5065A.

8-3. Shaded area on schematic diagrams indicate printed circuit board assemblies. Components within shaded areas are mounted on boards.

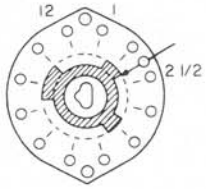
8-4. Theory and maintenance of assemblies is beside the schematic.

Figure 8-1. Schematic Diagram Notes

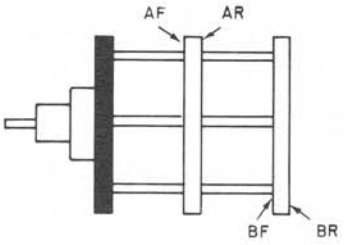
SYMBOLS

- FRONT PANEL
- REAR PANEL
- INTERIOR AND PC BOARDS
- WIPER MOVES TOWARD "CW" WHEN CONTROL IS ROTATED CLOCKWISE
- POWER LINE GROUND
- CIRCUIT COMMON GROUND
- FLOATING GROUND
- CHASSIS GROUND
- KNOB CONTROL
- SCREWDRIVER ADJUST
- MAIN SIGNAL PATH
- FEEDBACK PATH
- TEST POINT
- "AND" GATE
- "OR" GATE
- INVERTER
- NAND GATE
- NOR GATE
- EXCLUSIVE NOR

SWITCH DESIGNATIONS



A3S1		SWITCH S1 WITHIN ASSEMBLY A3
B		2ND WAFER FROM FRONT (A=1ST, ETC)
R		REAR OF WAFER (F=FRONT)
A3S1BR(2-1/2)	(2-1/2)	TERMINAL LOCATION ($2\frac{1}{2}$) (VIEWED FROM FRONT)



REFERENCE DESIGNATIONS

REFERENCE DESIGNATIONS WITHIN ASSEMBLIES ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION. JACKS ARE THE STATIONARY CONNECTORS AND PLUGS ARE THE MORE MOVEABLE OF TWO CONNECTORS.

ASSEMBLY	ABBREVIATION	COMPLETE DESCRIPTION
A25	C1	A25C1
A25A1	CR1	A25A1CR1
NO PREFIX	J3	J3

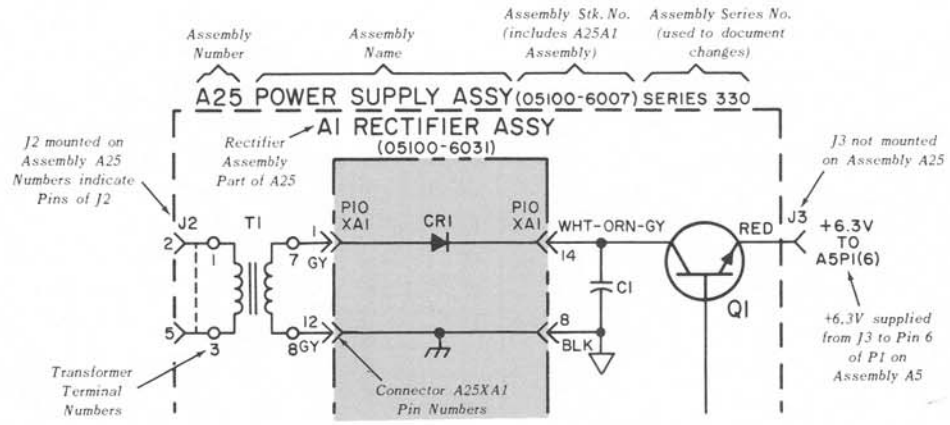
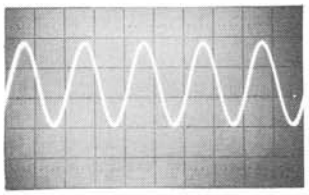
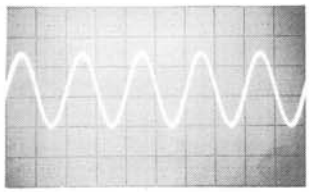


Figure 8-2
BLOCK DIAGRAM

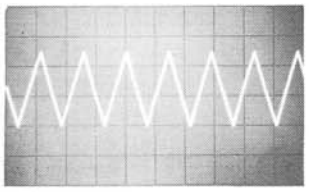
(See Page 8-3)



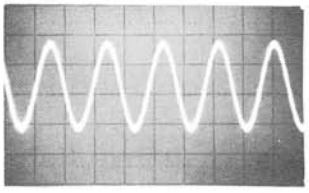
1 1 V/cm, .1 μs/cm
into 50Ω LOAD



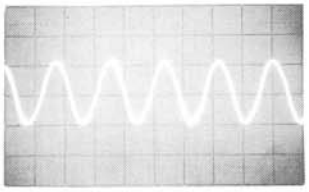
2 1 V/cm, .1 μs/cm



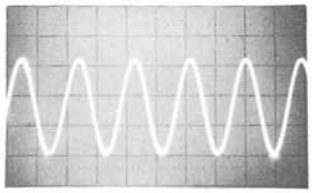
3 .5 V/cm, 5 ms/cm



4 .5 V/cm, .1 μs/cm

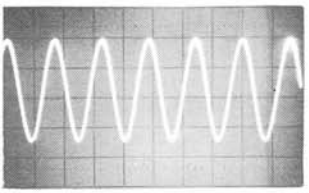


5 2 V/cm, 2 ms/cm

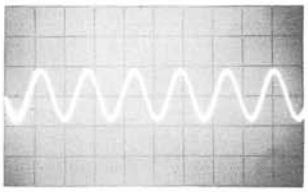


6 .5 V/cm, .1 μs/cm

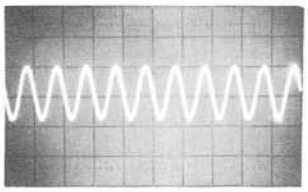
7 .5 V/cm, 2 ms/cm
LOOP OPEN OSC.
FINE at 300



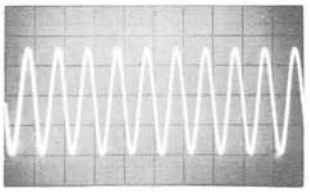
8 .5 V/cm, .1 ms/cm



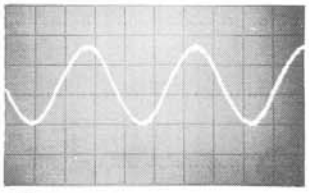
9 .5 V/cm, .1 ms/cm



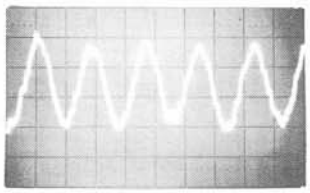
10 .5 V/cm, .1 μs/cm



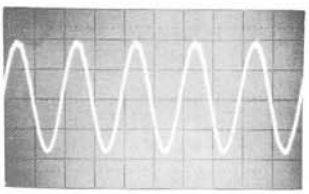
11 .5 V/cm, .1 μs/cm



12 .2 V/cm, 2 ms/cm
LOOP OPEN, OSC.
COARSE SET FOR
MAX SIGNAL

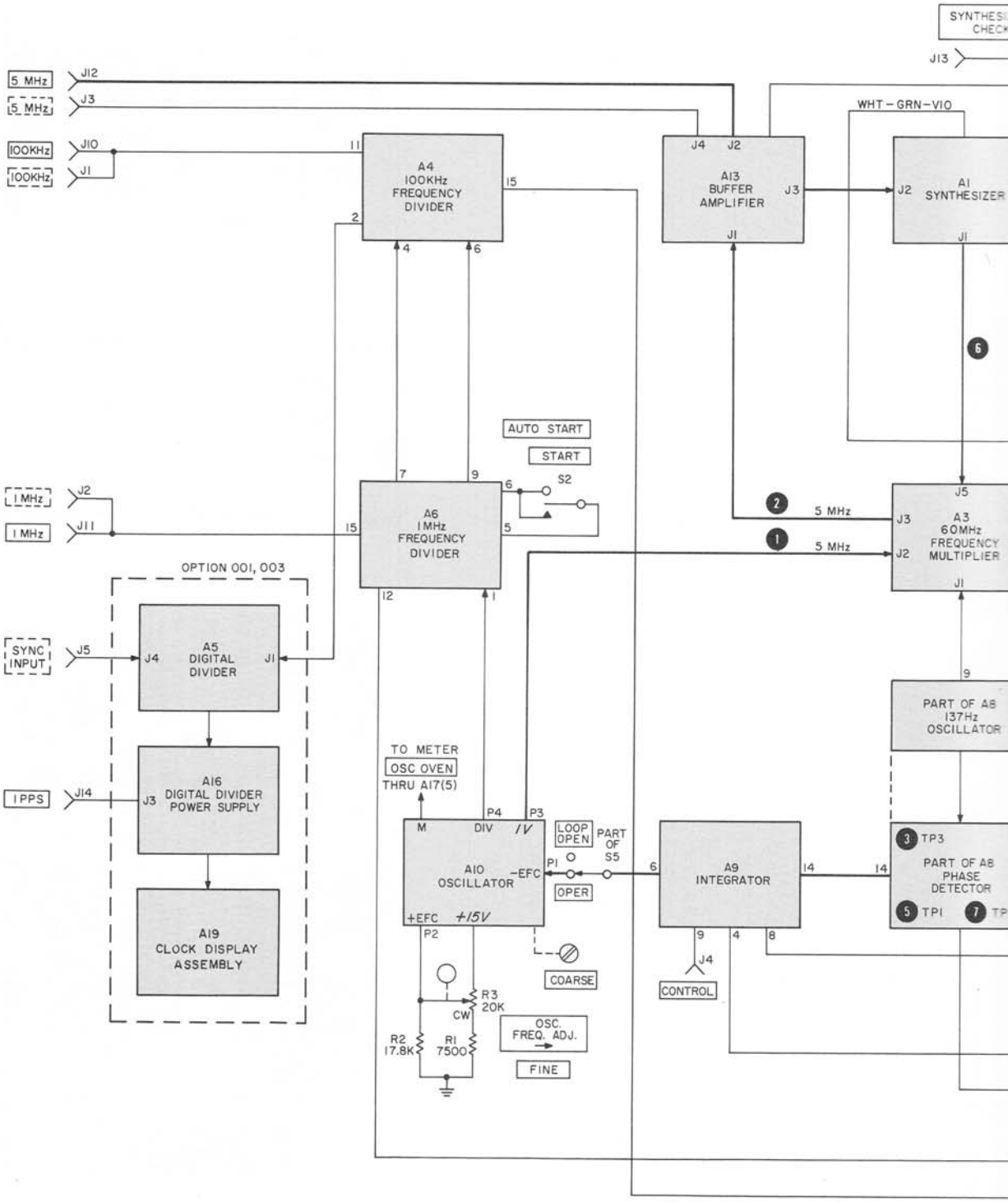


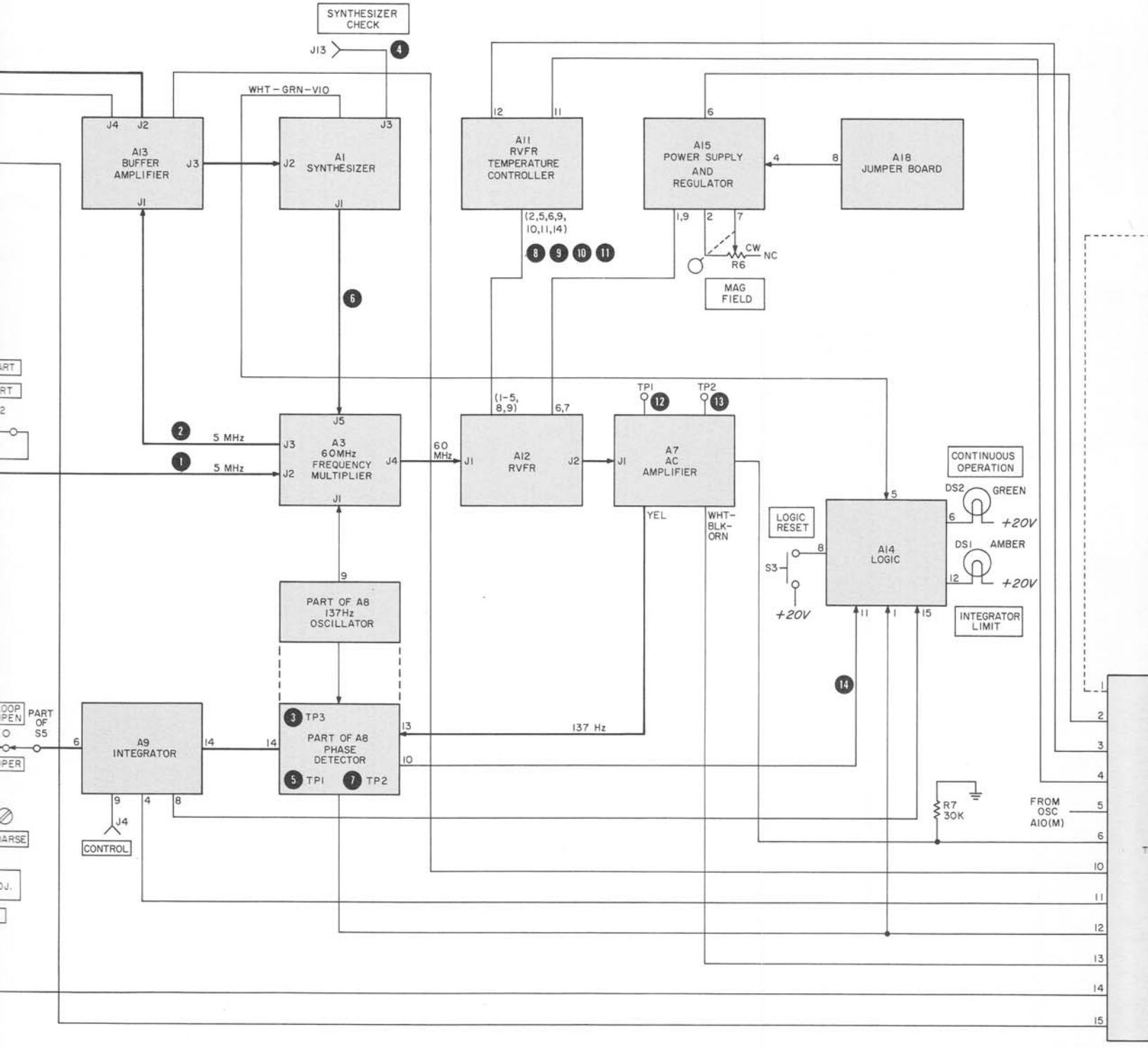
13 .05 V/cm, 2 μs/cm
LOOP OPEN, OSC.
COARSE SET FOR
MAX 2nd HARMONIC



14 .05 V/cm, .1 μs/cm

5065A: Normal operation unless noted.
Oscilloscope: DC coupled


SYNTHESI
CHECK
J13
5 MHz
J12
5 MHz
J3
100KHz
J10
100KHz
J1
A4
100KHz
FREQUENCY
DIVIDER
11
15
2
4
6
J4
J2
A13
BUFFER
AMPLIFIER
J3
J1
WHT-GRN-VIO
J2
A1
SYNTHESIZER
J1
6
AUTO START
START
S2
7
9
6
5
1 MHz
J2
1 MHz
J11
15
A6
1MHz
FREQUENCY
DIVIDER
2
5 MHz
1
5 MHz
J5
J3
A3
60MHz
FREQUENCY
MULTIPLIER
J2
J1
OPTION 001, 003
12
1
9
PART OF A8
137Hz
OSCILLATOR
SYNC
INPUT
J5
J4
A5
DIGITAL
DIVIDER
J1
TO METER
OSC OVEN
THRU A17(5)
1PPS
J14
J3
A16
DIGITAL DIVIDER
POWER SUPPLY
P4
P3
M
DIV 1V
LOOP
OPEN
PART
OF
S5
P1
A10
OSCILLATOR
-EFC
OPER
6
A9
INTEGRATOR
14
14
3 TP3
PART OF A8
PHASE
DETECTOR
5 TP1
7 TP
+EFC +15V
P2
9
4
8
J4
CONTROL
COARSE
R3
20K
CW
OSC.
FREQ. ADJ.
R2
17.8K
R1
7500
FINE
A19
CLOCK DISPLAY
ASSEMBLY


SYNTHESIZER CHECK
J13
4
WHT – GRN – VIO
A13 BUFFER AMPLIFIER
A1 SYNTHESIZER
A11 RVFR TEMPERATURE CONTROLLER
A15 POWER SUPPLY AND REGULATOR
A18 JUMPER BOARD
(2,5,6,9, 10,11,14)
8 9 10 11
CW
NC
R6
MAG FIELD
6
(1-5, 8,9)
6,7
TP1
TP2
12
13
2
5 MHz
1
5 MHz
A3 60MHz FREQUENCY MULTIPLIER
60 MHz
A12 RVFR
A7 AC AMPLIFIER
YEL
WHT-BLK-ORN
CONTINUOUS OPERATION
DS2
GREEN
+20V
LOGIC RESET
S3
+20V
A14 LOGIC
DS1
AMBER
+20V
INTEGRATOR LIMIT
14
PART OF A8 137Hz OSCILLATOR
9
PART OF S5
A9 INTEGRATOR
3 TP3
PART OF A8 PHASE DETECTOR
5 TP1
7 TP2
137 Hz
R7 30K
FROM OSC A1O(M)
J4
CONTROL
1
2
3
4
5
6
10
11
12
13
14
15

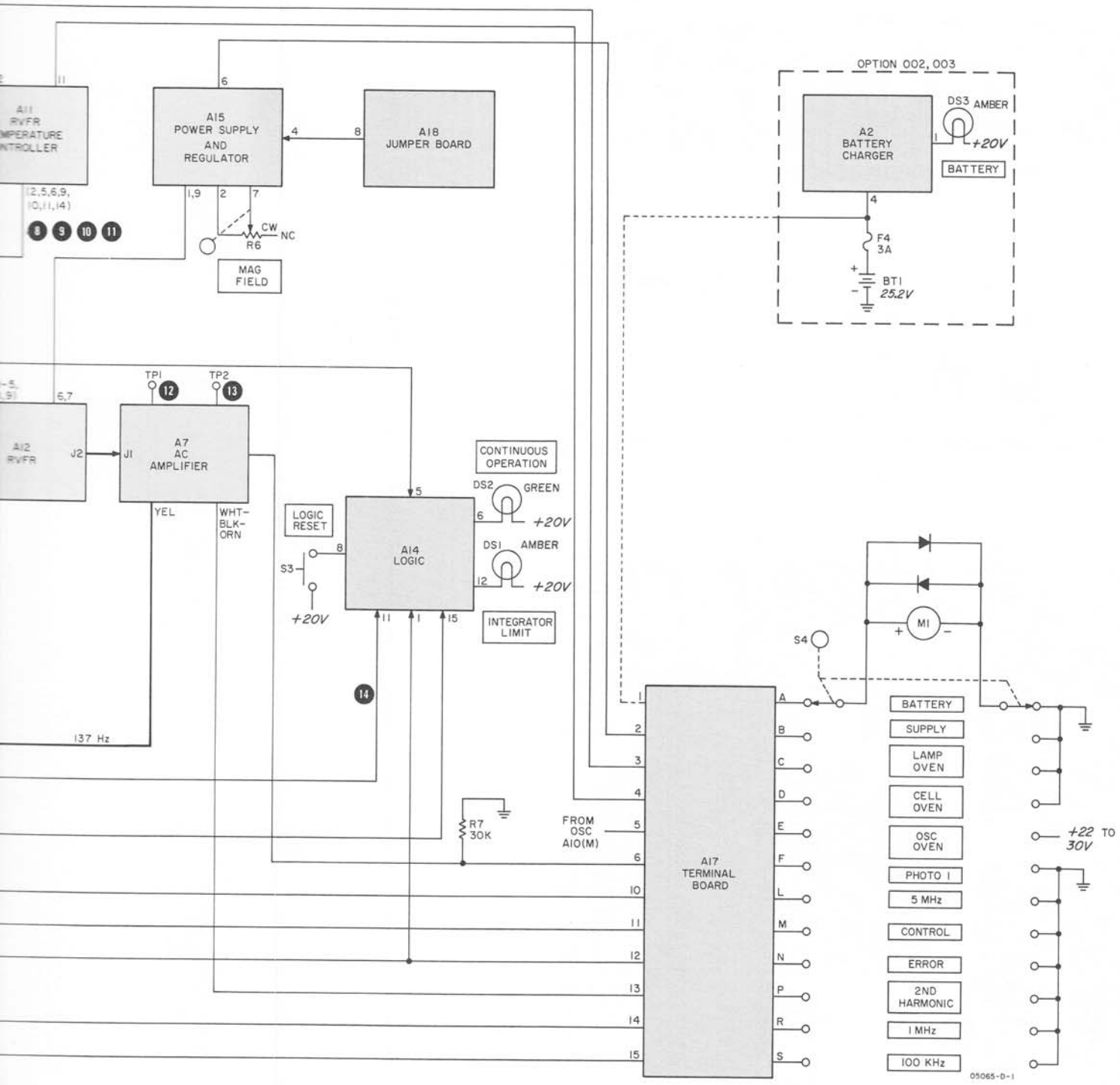


Figure 8-2. Block Diagram

Figure 8-3. Front and Rear Panel and Top Internal Views

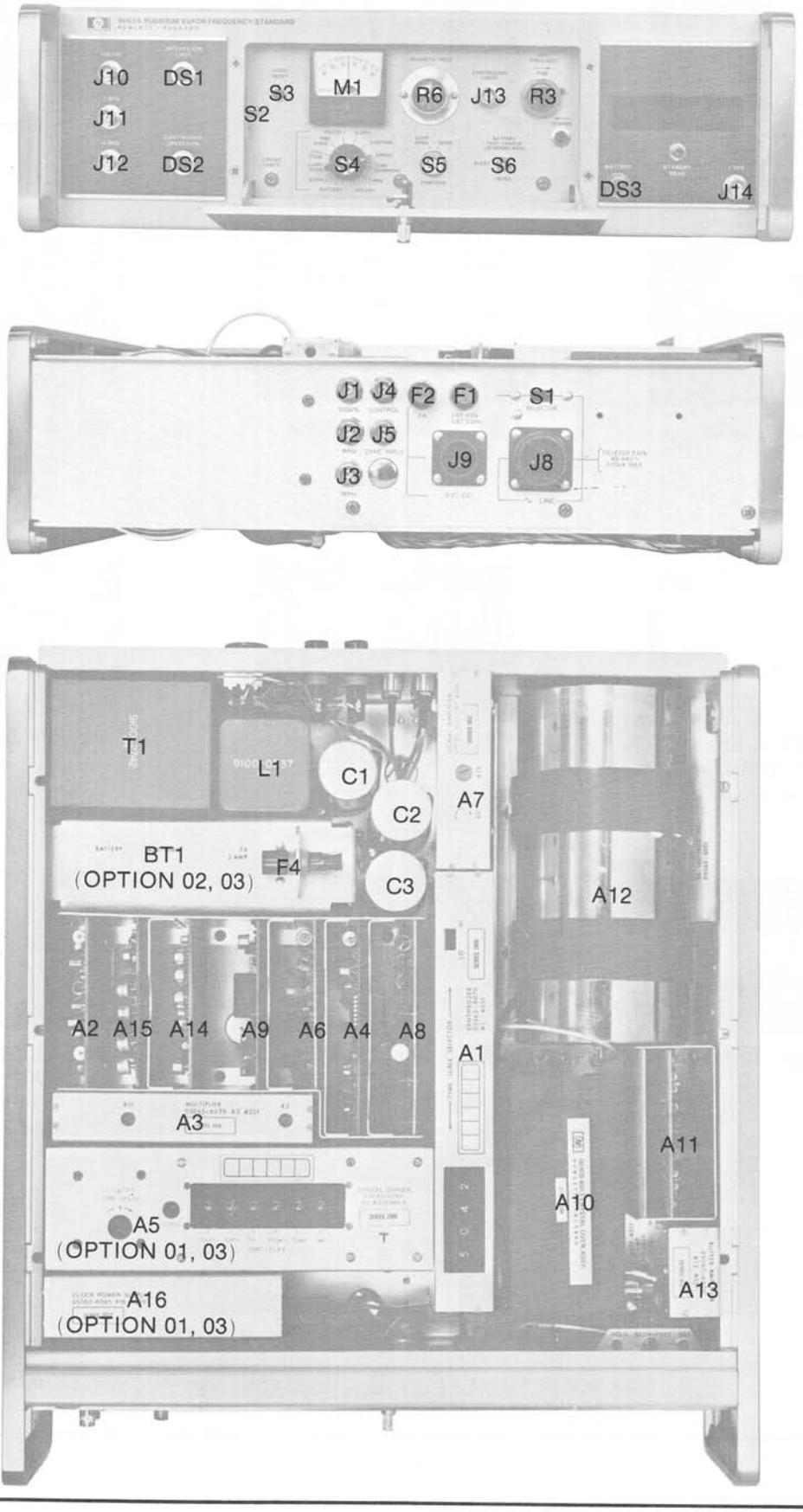
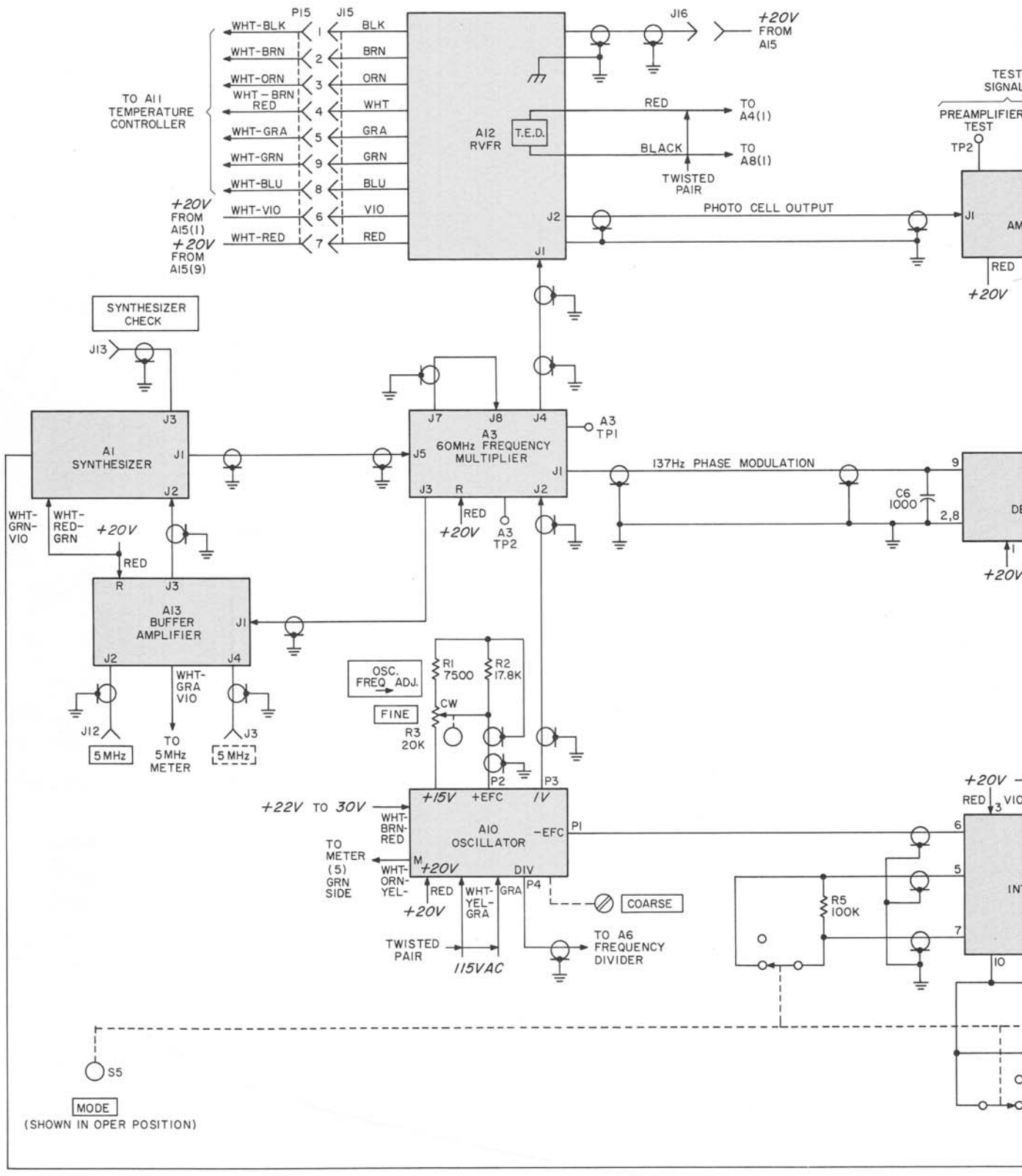


Figure 8-4
WIRING DIAGRAM (Sheet 1 of 3)

(See Page 8-5)


P15
J15
WHT-BLK
WHT-BRN
WHT-ORN
WHT-BRN
RED
WHT-GRA
WHT-GRN
WHT-BLU
WHT-VIO
WHT-RED
BLK
BRN
ORN
WHT
GRA
GRN
BLU
VIO
RED
TO A11 TEMPERATURE CONTROLLER
+20V FROM A15(1)
+20V FROM A15(9)
A12 RVFR
T.E.D.
J16
+20V FROM A15
RED
TO A4(1)
BLACK
TO A8(1)
TWISTED PAIR
PHOTO CELL OUTPUT
J2
J1
TEST SIGNAL
PREAMPLIFIER TEST
TP2
RED
+20V
SYNTHESIZER CHECK
J13
A1 SYNTHESIZER
J3
J1
J2
WHT-GRN-VIO
WHT-RED-GRN
+20V
RED
A3 60MHz FREQUENCY MULTIPLIER
J7
J8
J4
J5
J3
R
A3 TP1
137Hz PHASE MODULATION
C6 1000
2,8
9
1
+20V
RED
A3 TP2
A13 BUFFER AMPLIFIER
J2
J4
WHT-GRA VIO
J12
5MHz
TO 5MHz METER
J3
5MHz
OSC. FREQ. ADJ.
FINE
R1 7500
R2 17.8K
CW
R3 20K
P2
P3
+22V TO 30V
+15V
+EFC
-EFC
1V
A10 OSCILLATOR
P1
WHT-BRN-RED
TO METER (5) GRN SIDE
WHT-ORN-YEL-
M
+20V
DIV
P4
RED
WHT-YEL-GRA
GRA
+20V
TWISTED PAIR
115VAC
COARSE
TO A6 FREQUENCY DIVIDER
R5 100K
+20V
RED
VIO
3
6
5
7
10
S5
MODE
(SHOWN IN OPER POSITION)

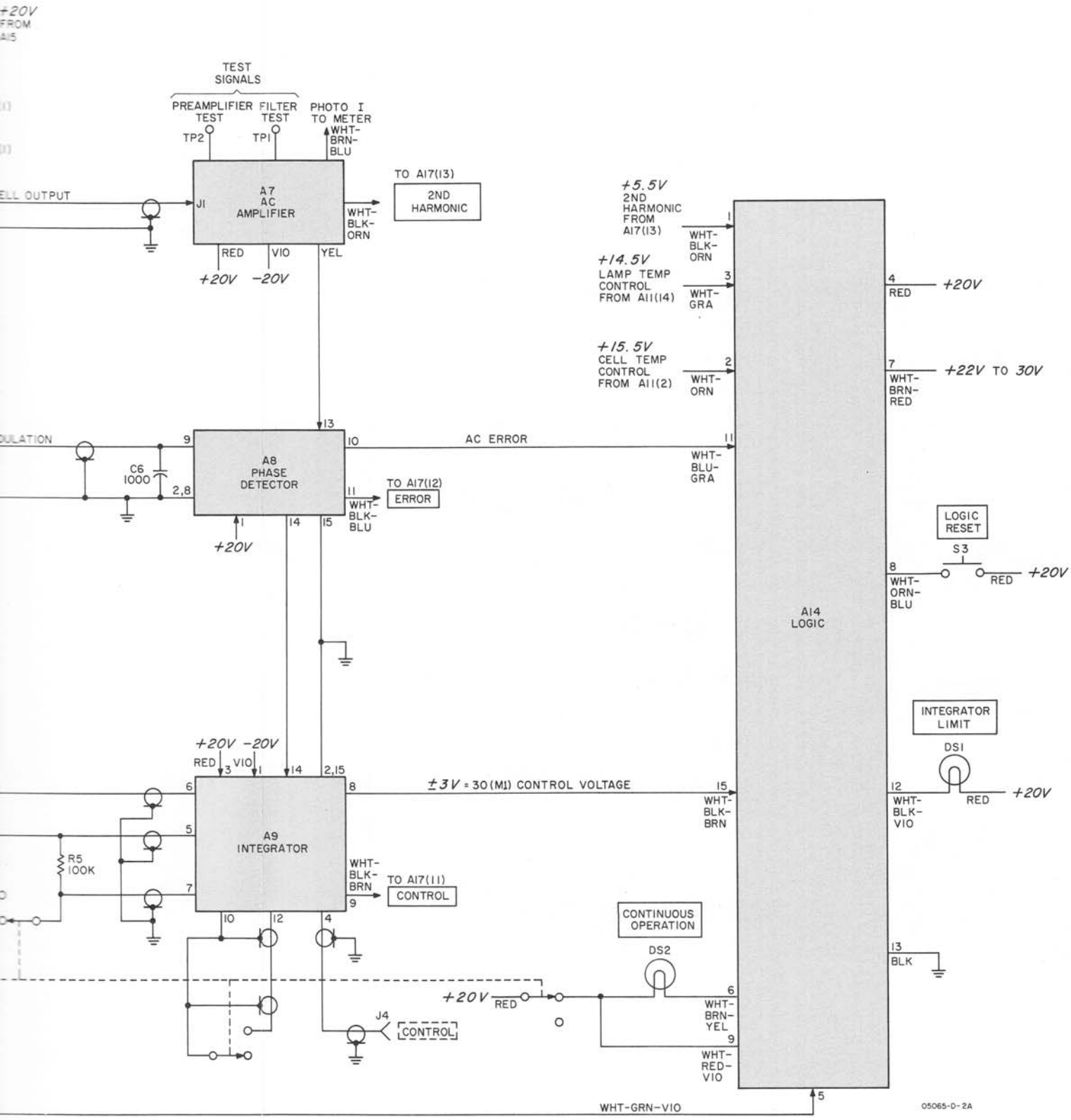


Figure 8-4. Wiring Diagram (Sheet 1 of 3)

Figure 8-5. Bottom Internal View

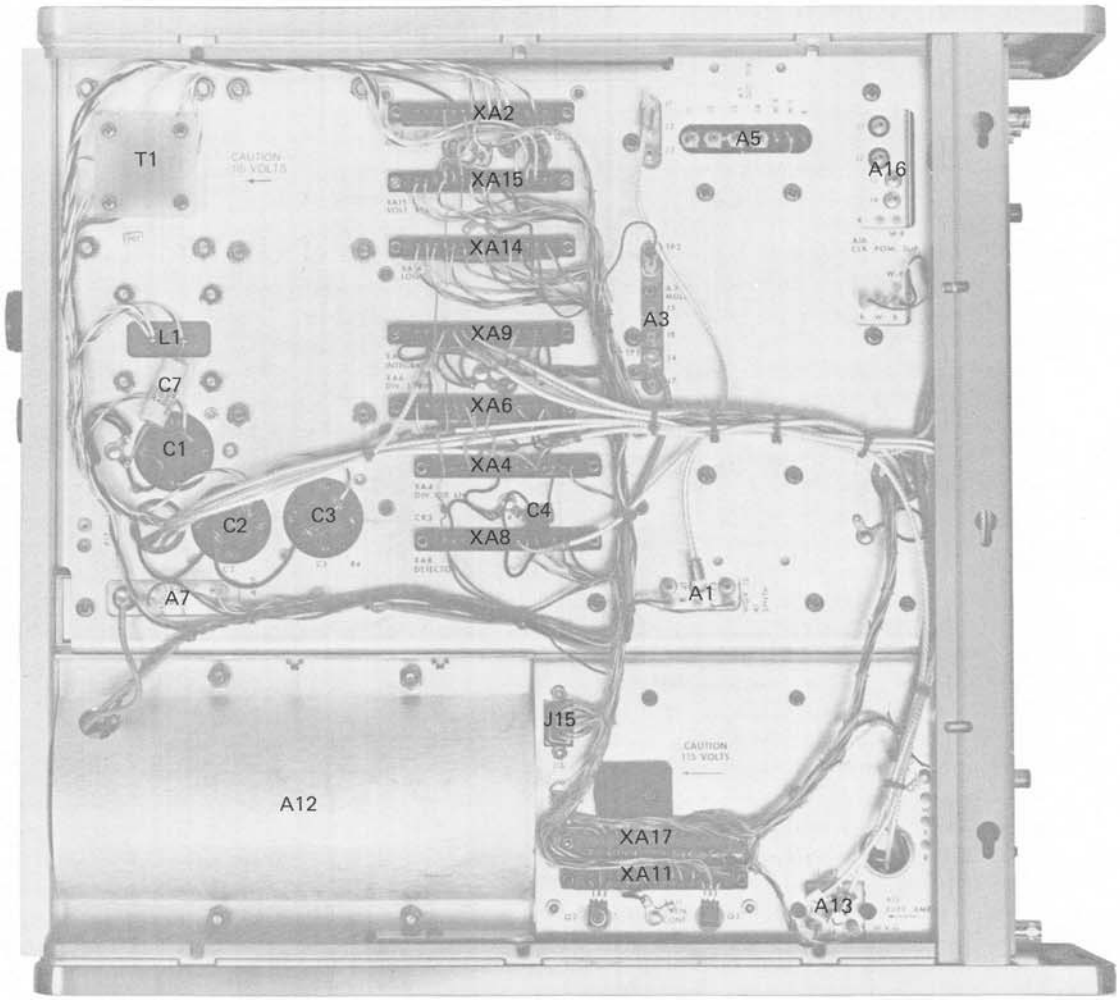
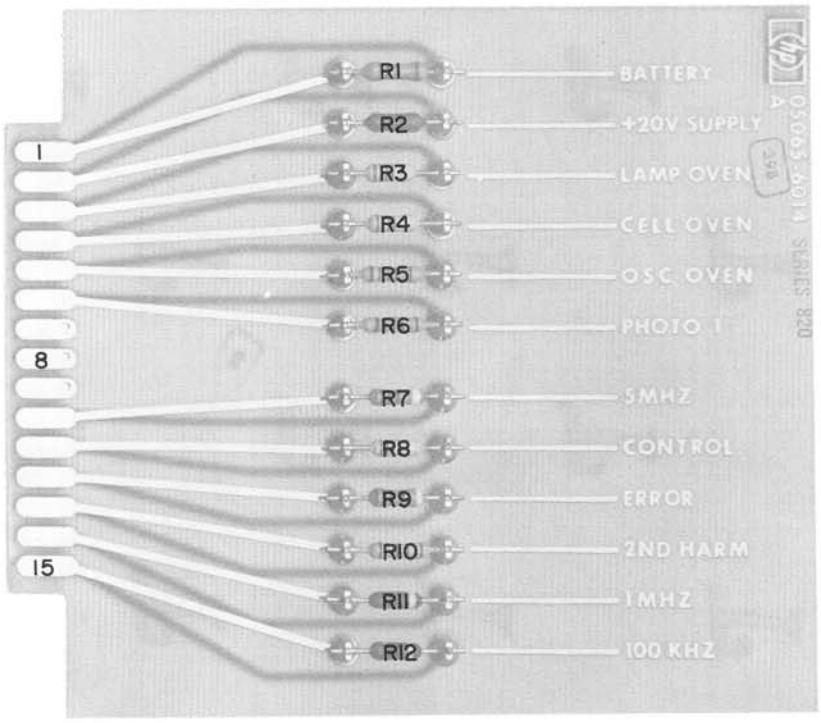


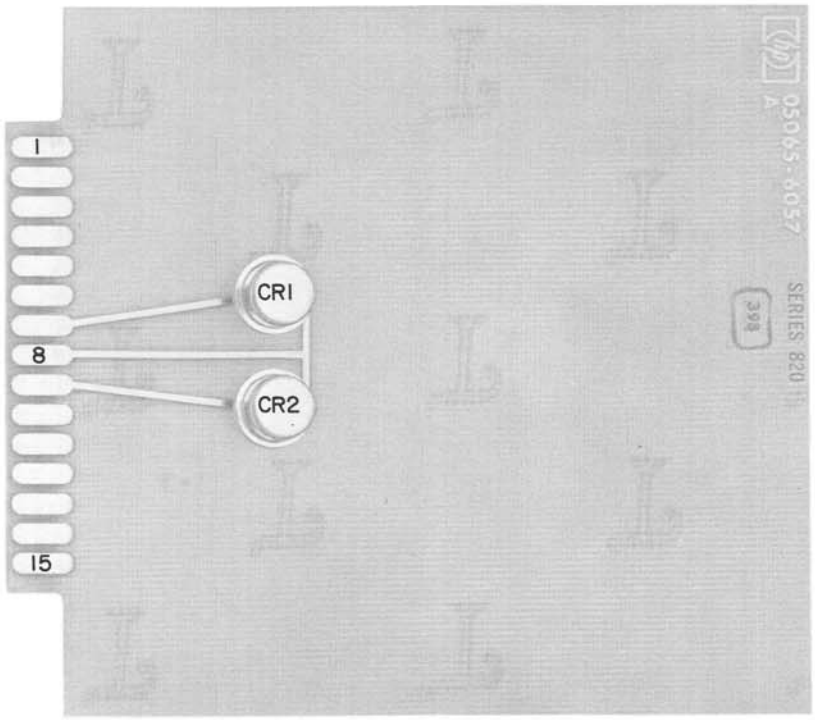
Figure 8-6
WIRING DIAGRAM (Sheet 2 of 3)

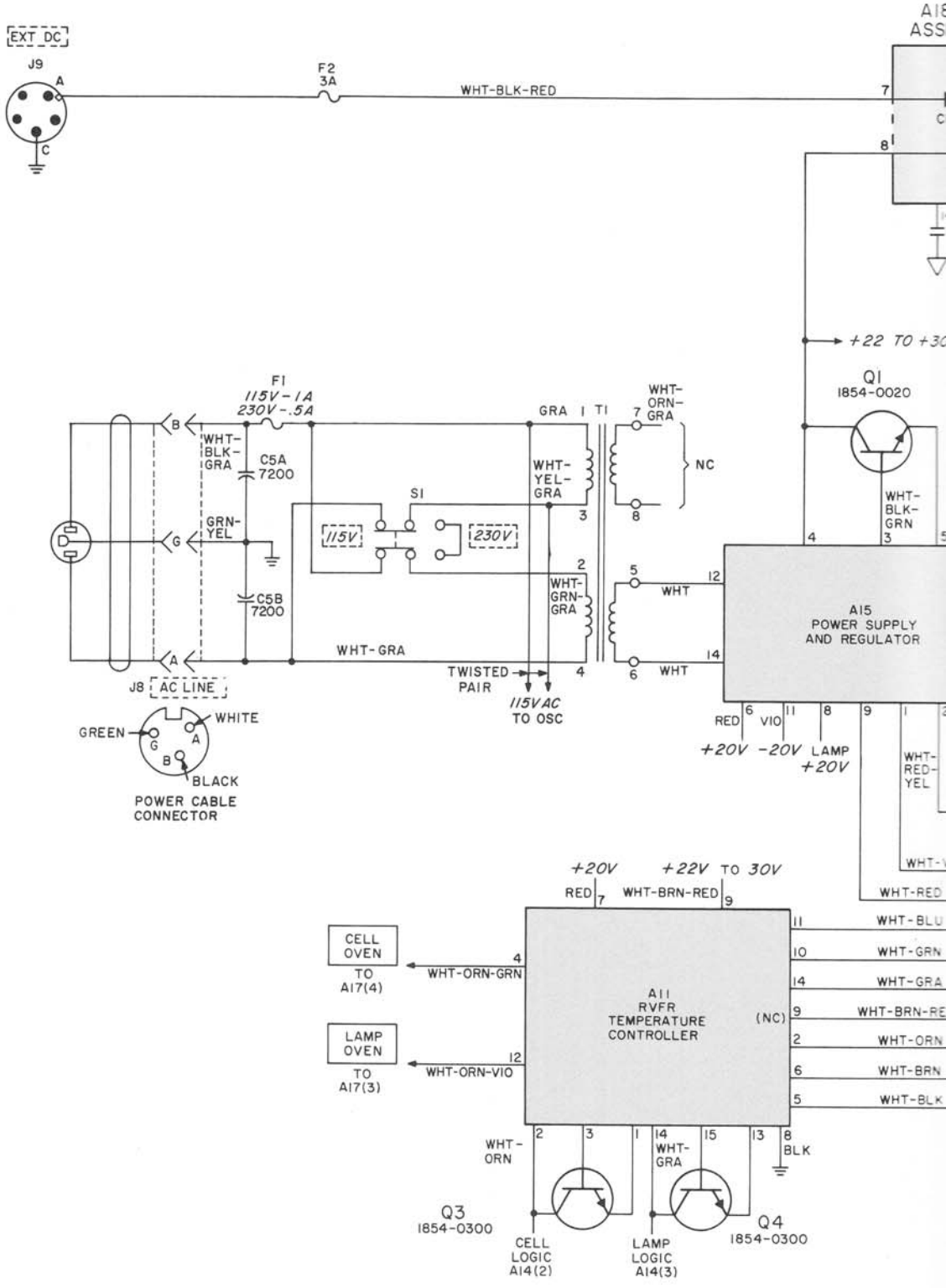
(See Page 8-7)

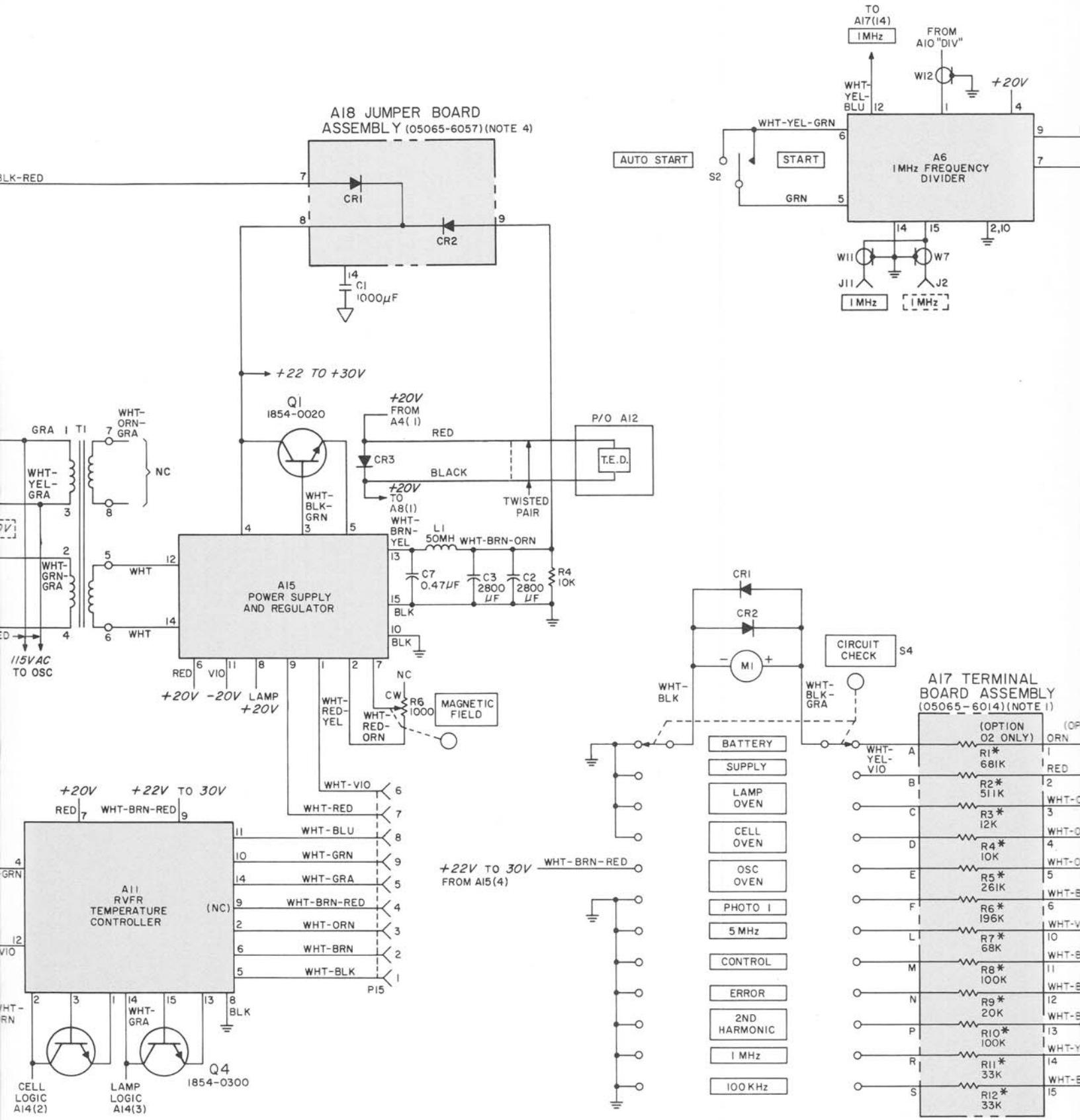
A17

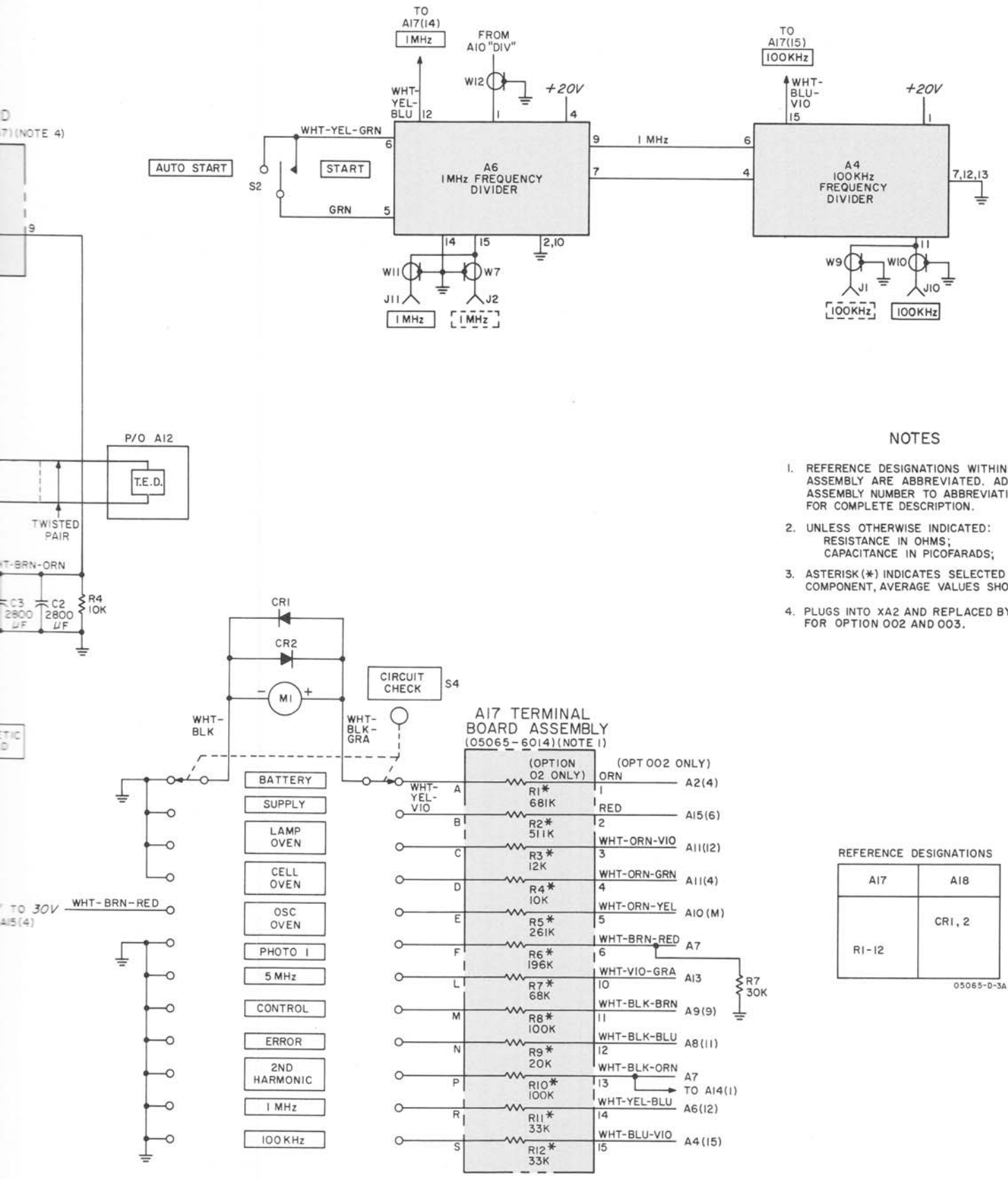

R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
1
8
15
BATTERY
+20V SUPPLY
LAMP OVEN
CELL OVEN
OSC OVEN
PHOTO 1
5MHZ
CONTROL
ERROR
2ND HARM
1MHZ
100 KHZ
05065-6014
SERIES 820

A18


1
8
15
CR1
CR2
05065-6057
SERIES 820


EXT DC
J9
A
C
F2
3A
WHT-BLK-RED
7
8
+22 TO +30
Q1
1854-0020
F1
115V-1A
230V-.5A
B
G
A
WHT-BLK-GRA
C5A
7200
GRN-YEL
C5B
7200
WHT-GRA
J8 AC LINE
GREEN
WHITE
BLACK
POWER CABLE CONNECTOR
GRA
T1
WHT-ORN-GRA
NC
WHT-YEL-GRA
S1
115V
230V
WHT-GRN-GRA
WHT
TWISTED PAIR
115VAC TO OSC
WHT-BLK-GRN
A15
POWER SUPPLY AND REGULATOR
RED
VIO
LAMP
+20V
-20V
+20V
+22V TO 30V
WHT-BRN-RED
WHT-RED-YEL
WHT-RED
CELL OVEN
TO A17(4)
WHT-ORN-GRN
LAMP OVEN
TO A17(3)
WHT-ORN-VIO
A11
RVFR
TEMPERATURE
CONTROLLER
(NC)
WHT-BLU
WHT-GRN
WHT-GRA
WHT-BRN-RE
WHT-ORN
WHT-BRN
WHT-BLK
WHT-ORN
WHT-GRA
BLK
Q3
1854-0300
Q4
1854-0300
CELL LOGIC A14(2)
LAMP LOGIC A14(3)


A18 JUMPER BOARD ASSEMBLY (05065-6057) (NOTE 4)
CR1
CR2
C1 1000μF
+22 TO +30V
Q1 1854-0020
+20V FROM A4(1)
CR3
RED
BLACK
P/O A12
T.E.D.
TWISTED PAIR
+20V TO A8(1)
WHT-BLK-GRN
WHT-BRN-YEL
L1 50MH
WHT-BRN-ORN
C7 0.47μF
C3 2800 μF
C2 2800 μF
R4 10K
A15 POWER SUPPLY AND REGULATOR
WHT-YEL-GRA
WHT-GRN-GRA
WHT-ORN-GRA
NC
WHT
115VAC TO OSC
RED +20V
VIO -20V
LAMP +20V
WHT-RED-YEL
WHT-RED-ORN
CW R6 1000
MAGNETIC FIELD
TO A17(14) 1MHz
FROM A10 "DIV"
W12
+20V
WHT-YEL-BLU
WHT-YEL-GRN
AUTO START
START
S2
GRN
A6 1MHz FREQUENCY DIVIDER
W11
W7
J11
J2
1MHz
CIRCUIT CHECK
S4
M1
WHT-BLK
WHT-BLK-GRA
BATTERY
SUPPLY
LAMP OVEN
CELL OVEN
OSC OVEN
PHOTO 1
5 MHz
CONTROL
ERROR
2ND HARMONIC
1 MHz
100 KHz
+22V TO 30V FROM A15(4)
WHT-BRN-RED
A17 TERMINAL BOARD ASSEMBLY (05065-6014) (NOTE 1)
(OPTION 02 ONLY)
R1* 681K
R2* 511K
R3* 12K
R4* 10K
R5* 261K
R6* 196K
R7* 68K
R8* 100K
R9* 20K
R10* 100K
R11* 33K
R12* 33K
WHT-YEL-VIO
A11 RVFR TEMPERATURE CONTROLLER
+20V
+22V TO 30V
RED
WHT-BRN-RED
WHT-VIO
WHT-RED
WHT-BLU
WHT-GRN
WHT-GRA
WHT-BRN-RED
WHT-ORN
WHT-BRN
WHT-BLK
P15
BLK
CELL LOGIC A14(2)
LAMP LOGIC A14(3)
Q4 1854-0300



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS;
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN
4. PLUGS INTO XA2 AND REPLACED BY A2 FOR OPTION 002 AND 003.

REFERENCE DESIGNATIONS

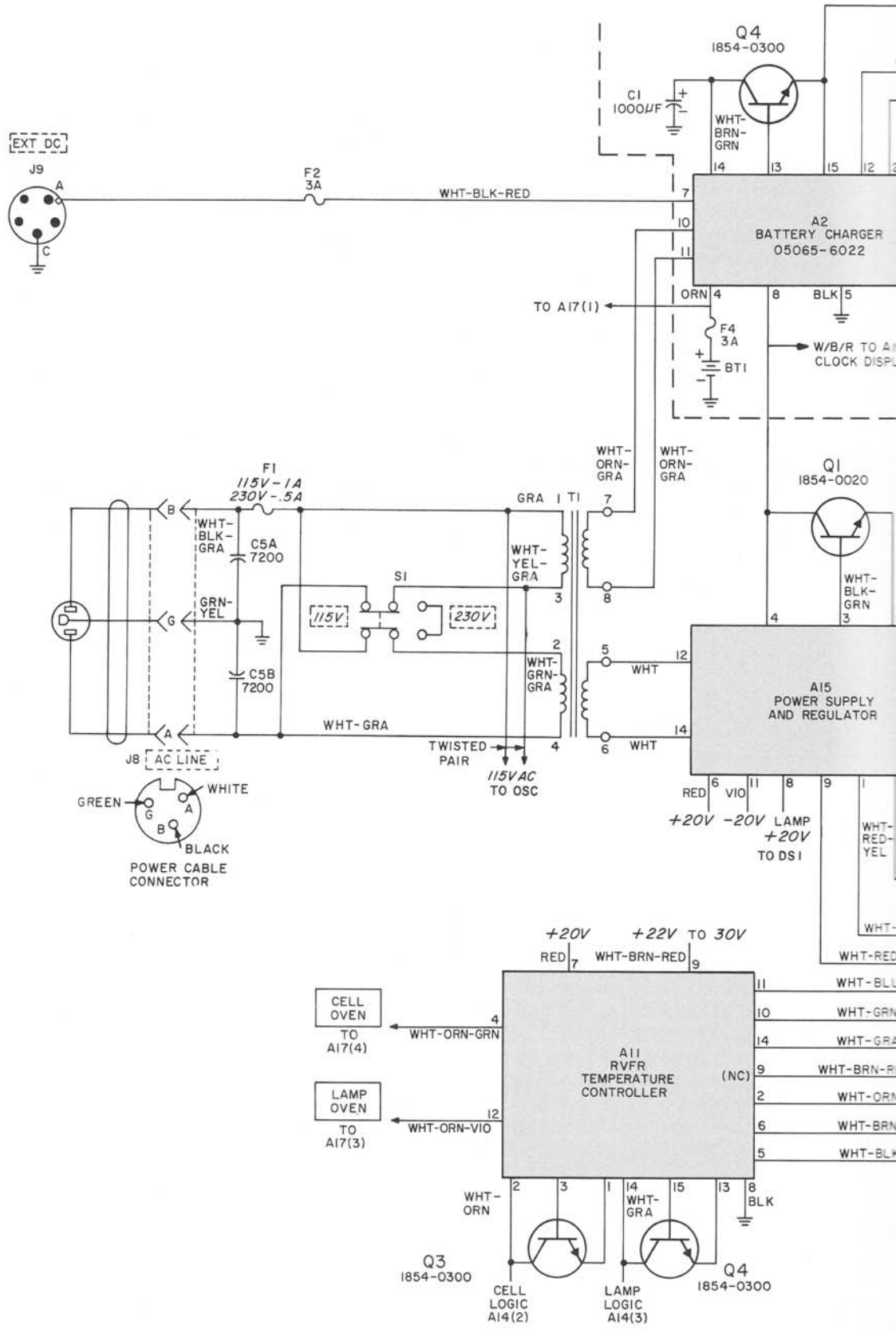
A17	A18
R1-12	CR1, 2

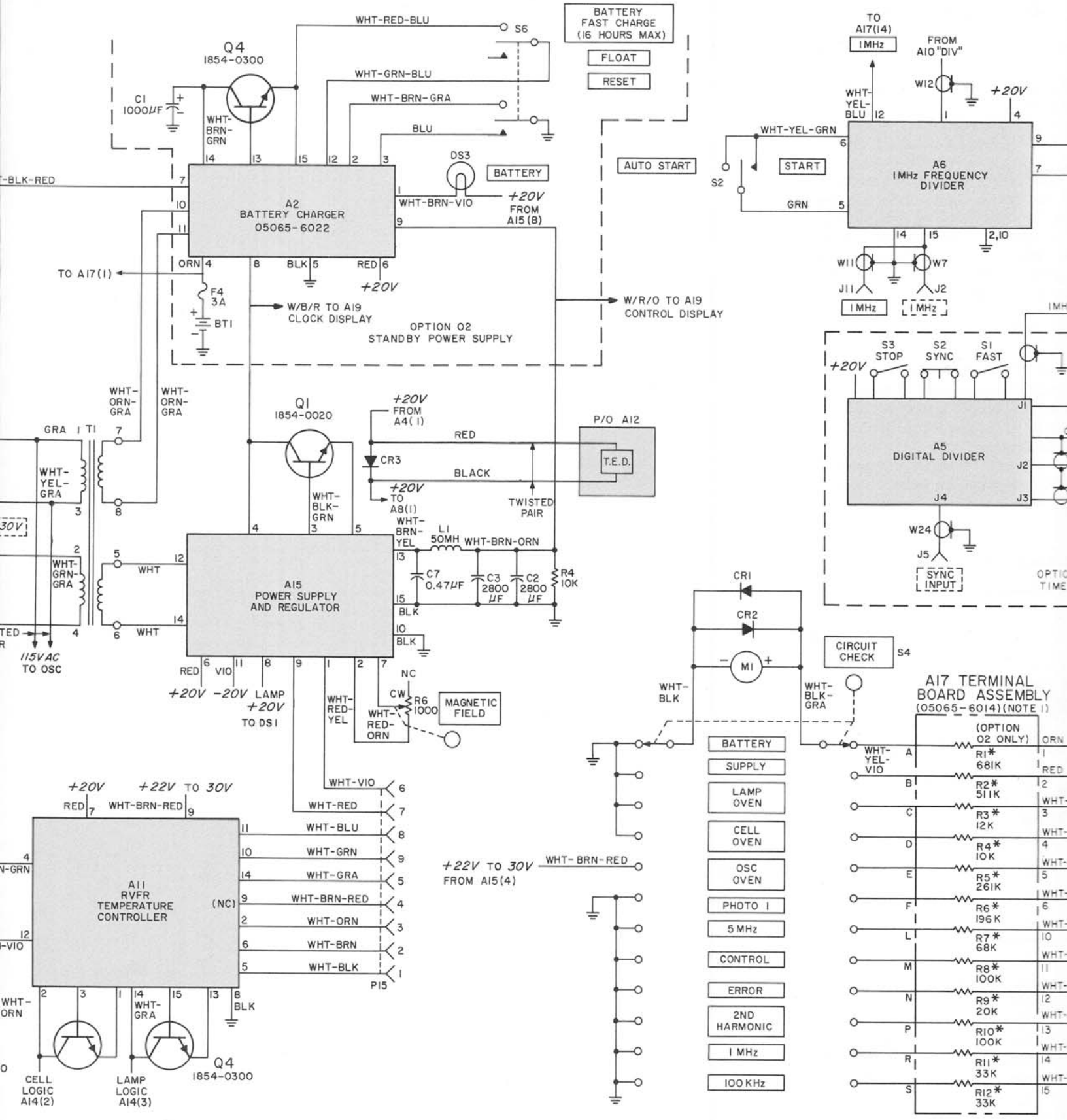
05065-D-3A

Figure 8-6. Wiring Diagram (Sheet 2 of 3)

Figure 8-7
WIRING DIAGRAM (Sheet 3 of 3)

(See Page 8-9)


Q4
1854-0300
C1
1000μF
WHT-
BRN-
GRN
EXT DC
J9
A
C
F2
3A
WHT-BLK-RED
A2
BATTERY CHARGER
05065-6022
TO A17(1)
ORN
BLK
F4
3A
BT1
W/B/R TO A
CLOCK DISP
F1
115V-1A
230V-.5A
WHT-
BLK-
GRA
C5A
7200
GRN-
YEL
C5B
7200
S1
115V
230V
GRA
T1
WHT-
YEL-
GRA
WHT-
GRN-
GRA
WHT-GRA
TWISTED
PAIR
115VAC
TO OSC
WHT-
ORN-
GRA
WHT-
ORN-
GRA
Q1
1854-0020
WHT-
BLK-
GRN
WHT
WHT
A15
POWER SUPPLY
AND REGULATOR
J8
AC LINE
GREEN
WHITE
BLACK
POWER CABLE
CONNECTOR
RED
VIO
LAMP
+20V
-20V
+20V
TO DS1
WHT-
RED-
YEL
+20V
+22V TO 30V
RED
WHT-BRN-RED
CELL
OVEN
TO
A17(4)
WHT-ORN-GRN
LAMP
OVEN
TO
A17(3)
WHT-ORN-VIO
A11
RVFR
TEMPERATURE
CONTROLLER
(NC)
WHT-BLU
WHT-GRN
WHT-GRA
WHT-BRN-R
WHT-ORN
WHT-BRN
WHT-BLK
WHT-
ORN
WHT-
GRA
BLK
Q3
1854-0300
Q4
1854-0300
CELL
LOGIC
A14(2)
LAMP
LOGIC
A14(3)


BATTERY FAST CHARGE (16 HOURS MAX)
FLOAT
RESET
AUTO START
BATTERY
S6
S2
START
Q4
1854-0300
C1
1000µF
WHT-BRN-GRN
WHT-RED-BLU
WHT-GRN-BLU
WHT-BRN-GRA
BLU
DS3
WHT-BRN-VIO
+20V FROM A15(8)
A2
BATTERY CHARGER
05065-6022
TO A17(1)
F4
3A
BT1
W/B/R TO A19
CLOCK DISPLAY
OPTION 02
STANDBY POWER SUPPLY
W/R/O TO A19
CONTROL DISPLAY
TO A17(14)
1MHz
FROM A10 "DIV"
W12
WHT-YEL-BLU
WHT-YEL-GRN
GRN
A6
1MHz FREQUENCY DIVIDER
W11
W7
J11
J2
1MHz
S3 STOP
S2 SYNC
S1 FAST
A5
DIGITAL DIVIDER
J1
J2
J4
J3
W24
J5
SYNC INPUT
Q1
1854-0020
+20V FROM A4(1)
CR3
RED
BLACK
P/O A12
T.E.D.
TWISTED PAIR
+20V TO A8(1)
WHT-ORN-GRA
GRA
WHT-YEL-GRA
WHT-GRN-GRA
WHT-BLK-GRN
WHT-BRN-YEL
L1
50MH
WHT-BRN-ORN
C7
0.47µF
C3
2800 µF
C2
2800 µF
R4
10K
A15
POWER SUPPLY AND REGULATOR
WHT
BLK
115VAC TO OSC
RED
VIO
+20V
-20V
LAMP +20V TO DS1
WHT-RED-YEL
WHT-RED-ORN
NC
CW
R6
1000
MAGNETIC FIELD
CR1
CR2
M1
CIRCUIT CHECK
S4
WHT-BLK
WHT-BLK-GRA
A17 TERMINAL BOARD ASSEMBLY
(05065-6014)(NOTE 1)
(OPTION 02 ONLY)
WHT-YEL-VIO
R1* 681K
R2* 511K
R3* 12K
R4* 10K
R5* 261K
R6* 196K
R7* 68K
R8* 100K
R9* 20K
R10* 100K
R11* 33K
R12* 33K
BATTERY
SUPPLY
LAMP OVEN
CELL OVEN
OSC OVEN
PHOTO 1
5 MHz
CONTROL
ERROR
2ND HARMONIC
1 MHz
100 KHz
+22V TO 30V
WHT-BRN-RED
FROM A15(4)
+20V
+22V TO 30V
RED
WHT-BRN-RED
A11
RVFR
TEMPERATURE
CONTROLLER
(NC)
WHT-VIO
WHT-RED
WHT-BLU
WHT-GRN
WHT-GRA
WHT-BRN-RED
WHT-ORN
WHT-BRN
WHT-BLK
P15
WHT-ORN
WHT-GRA
BLK
CELL LOGIC A14(2)
LAMP LOGIC A14(3)
Q4
1854-0300

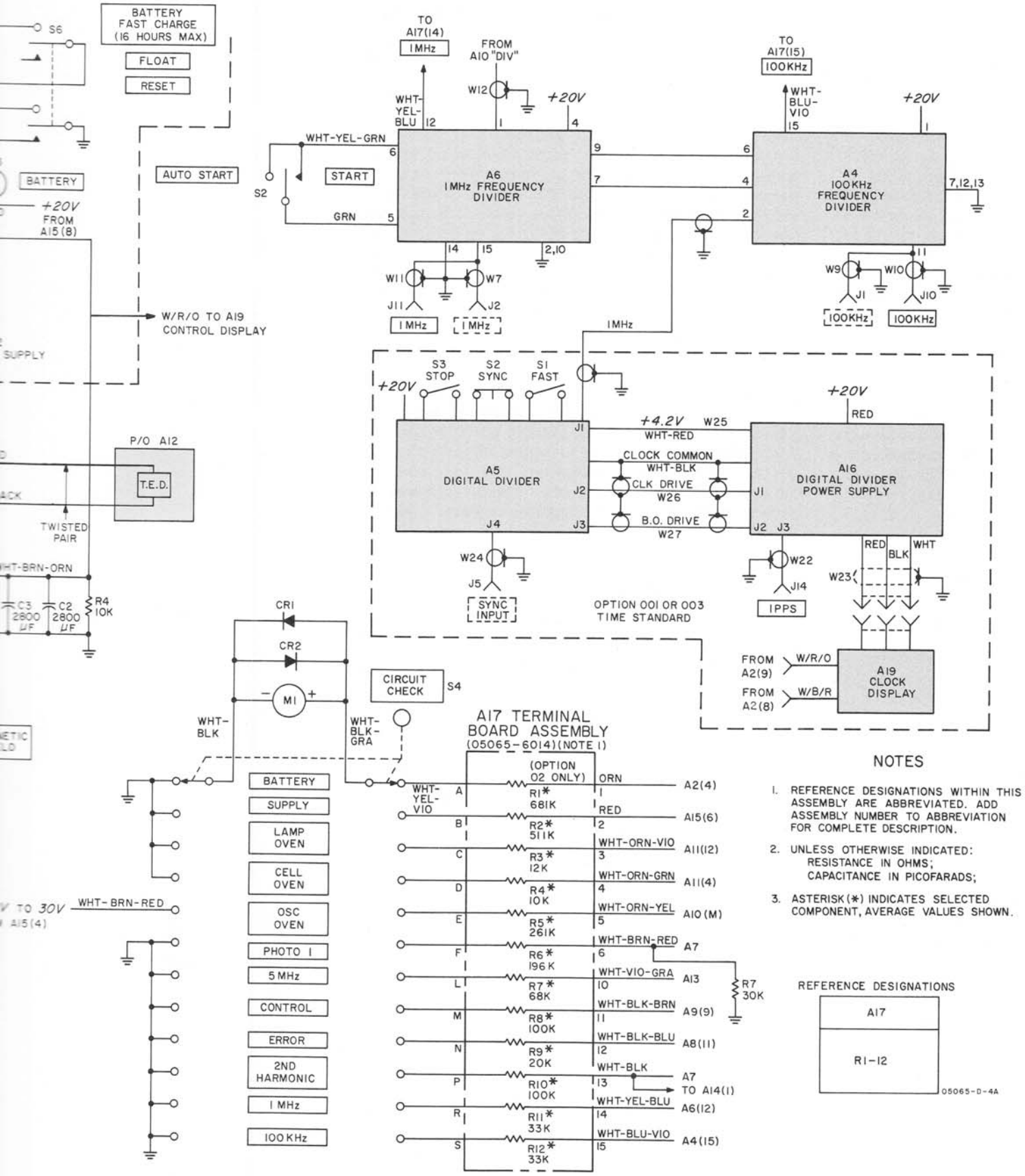


Figure 8-7. Wiring Diagram (Sheet 3 of 3)

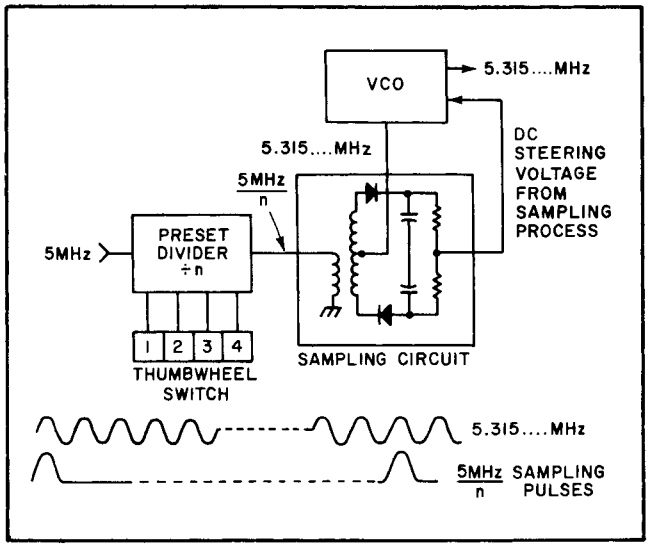
UNIT THEORY OF OPERATION

Synthesizer Assembly A1

Synthesizer Assembly A1 produces a 5.315...MHz signal that is mixed with 6840 MHz in a step-recovery diode producing the 6,834,685 Hz microwave field which excites the rubidium vapor cell in a resonant microwave cavity of RVFR Assembly A12. Synthesizer frequency is adjustable by the TIME SCALE thumbwheel switches and the HI/LO slide switch on A1 Assembly. (These controls can be seen with the unit top cover removed.) Output frequencies corresponding to thumbwheel and slide switch settings are in Table 3-6 under OPERATION. The thumbwheel switch setting for A1 operation is listed on the RVFR decal (for access, remove 5065A top cover). The thumbwheel switch setting for UTC (Universal Time) is listed on the front panel door.

The following illustration shows the synthesizing technique for the required 5.315...MHz output. The 5 MHz input is first digitally divided in the preset divider according to the setting of th thumbwheel switches to produce the "n" of the rational fraction m/n which expresses the multiplier ratio for the required synthesizer output. Preset divider output pulses are first sharpened in a blocking oscillator; then applied to a harmonic sampler circuit.

Synthesizer Multiplication Technique



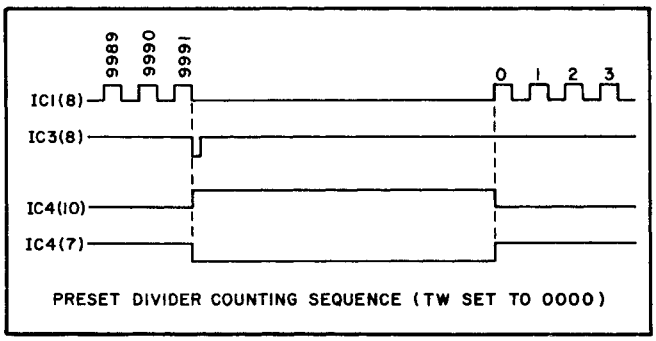
In the harmonic sampler circuit, the 5 MHz/n frequency is compared with the nominal 5.315 MHz frequency of the voltage controlled oscillator. This action produces a dc steering voltage which controls the variable frequency oscillator to synchronize its "m" harmonic with the 5 MHz/n division, thus producing harmonic m of the rational fraction m/n. In this manner, the thumbwheel switches set the desired output frequency. The 5.315...MHz output signal is available as a test signal at the SYNTHESIZER CHECK jack on the front panel.

THE PRESET DIVIDER

The preset divider is made up of four decades giving a total dividing capability of 10,000. With each 10,000 counts applied to the divider input, there will be one output pulse. With the addition of the preset capability this divider can be set to divide by any integer (except 1 through 9, due to preset time). Since the divider can be set to divide by any predetermined integer, the system is considered a divide-by-n preset divider. For example; if the divider were to divide-by-2, an 8 would be preset into the decade before the counting sequence starts, and since an 8 count is already in the decade from the preset, it will take only 2 inputs to get 1 output. Conversely, to divide-by-8, 2 counts are preset into the decade prior to counting.

The preset divider delivers an "H" output to the sample circuit starting at count 9991 and holding thru count 9999. During this time the input gate Q3 closes to prevent 5 MHz pulse train from entering the decades during preset. The preset number is determined by four thumbwheel switches. At the same time that IC4 delivers an "H" output to the sample circuit it supplies a preset pulse to the decades IC1(1), IC2(1), IC5(1), and IC6(1). At the end of the preset period gate Q3 opens and counting resumes until 9991 is obtained again.

Synthesizer Assembly Timing Diagram



The 5 MHz input signal is shaped by amplifier Q2. The pulses are then applied to decade IC1(8). The decades are connected in series. The sensing gate IC3 detects when count reaches 9991 by sensing nines in IC2, 5, 6, and a one in IC1. The IC3 output then triggers the one-shot IC4. The duration of the one-shot output is approximately 1.8 μsec. During the 1.8 μsecs the decades are preset by the pulse output of IC4(7). At the end of 1.8 sec the decades are preset and ready to resume counting. By sensing nine counts ahead, sufficient time is available to preset the decades to any integer "n", from 1 to 9990.

POWER SUPPLY CIRCUITS

A regulated +5 V supply, obtained from the +20 V supply, is provided for the preset divider circuits. Reference diode CR1 and regulator Q1 maintain a constant +5 V supply to the preset divider.

Figure 8-8
SYNTHESIZER ASSEMBLY A1 BLOCK DIAGRAM
DIGITAL SECTION

(See Page 8-11)

MAINTENANCE

Synthesizer Assembly A1

NORMAL OPERATION

The A1 Synthesizer Assembly processes 5 MHz to produce the required 5.315...MHz. This is added to the A3 Multiplier 60 MHz output and multiplied to 6,834,685 Hz by the step-recovery diode in the RVFR Assembly. To obtain proper Synthesizer output frequencies for UTC and A1 operation, the Synthesizer output is adjustable by the TIME SCALE slide switch and thumbwheel switch located under the top cover of the 5065A. Output frequencies corresponding to all the TIME SCALE settings can be found in Table 3-6 of OPERATION. The thumbwheel switch setting for A1 operation is listed in the RVFR decal. The thumbwheel switch setting for UTC operation is listed on the front panel door.

PERFORMANCE CHECK

If trouble is suspected in the A1 Synthesizer Assembly, the following checks will verify proper or improper operation.

a. Phase Lock Check. Remove top and bottom covers. Connect an oscilloscope to A1TP1 (on bottom of instrument). If the waveform is a random AC signal then the phase-locked oscillator section of the Synthesizer is out of lock. Check thumbwheel and HI/LO switch settings to be sure they are correct. If these switch settings are OK, troubleshoot Synthesizer circuit as described under A1 Troubleshooting. If signal at A1TP1 is correct, check Synthesizer output frequencies versus the thumbwheel settings as described in the following paragraph.

b. Synthesizer Frequency Check. Set up 5065A, frequency counter, and RF voltmeter as shown in Figure 2.

Note thumbwheel and HI/LO switch settings on A1 Synthesizer Assembly. Go to Table 3-6 in OPERATION and determine the frequency corresponding to these settings. The counter should read this frequency ±1 count. The RF voltmeter should indicate 100 mV rms or more. If the counter and RF voltmeter readings are correct, the Synthesizer is working properly at this setting.

A further check of Synthesizer operation at several points over its operating range can be made by setting the switches and reading the frequencies shown in the table below. All frequency readings should be within ±1 count; RF voltmeter should read 100 mV or greater.

Thumbwheel Switch Setting	HI/LO Switch	Frequency (Hz)
9000	HI	5315000.0
9159	HI	5315101.1
9635	HI	5315068.5
8714	HI	5314930.0
9603	HI	5314861.5
9047	HI	5314795.4
8777	HI	5314700.7
8697	LO	5314658.5
9253	LO	5314591.7
8919	LO	5314523.6
7758	LO	5314451.4
9348	LO	5314417.2

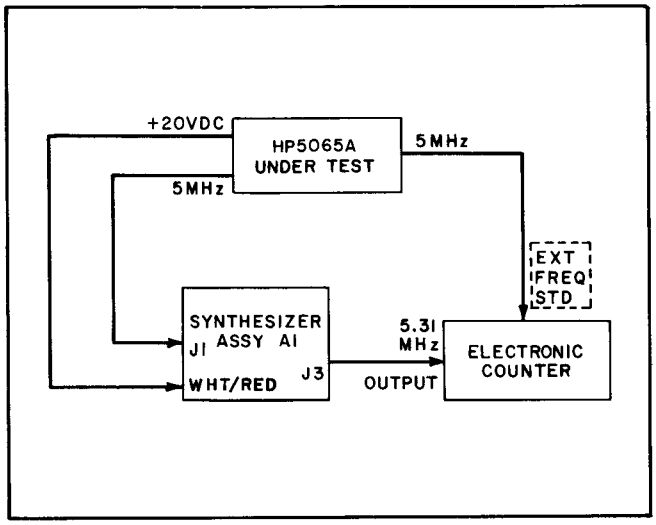
NOTE

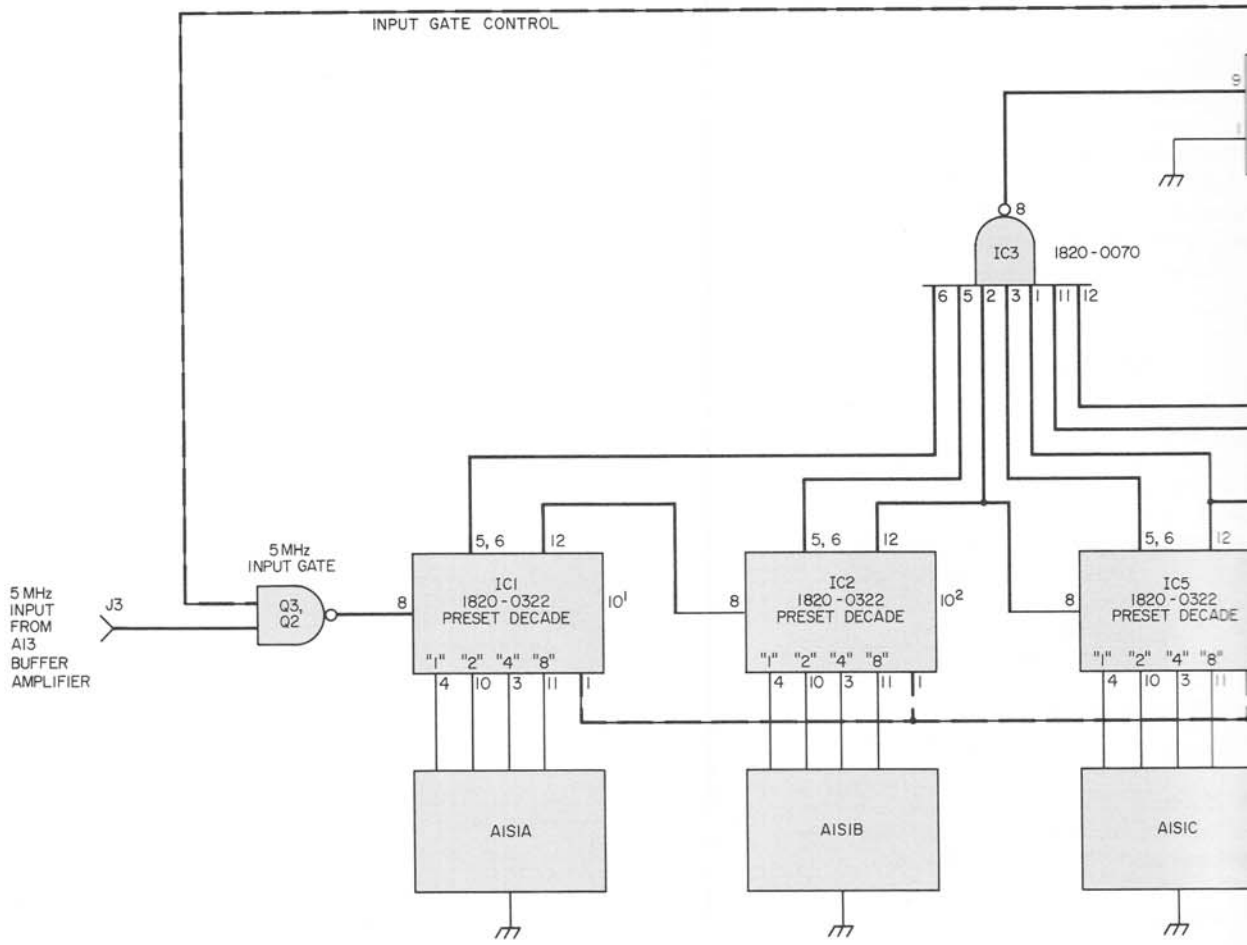
If the thumbwheel switches are changed from one setting to another or service is performed on A1, allow at least 1 minute of recovery time before attempting to get the continuous operation lamp to light.

TROUBLESHOOTING (See Figure 1).

To check out the Synthesizer circuits, pull off the electrical snap-on connectors and remove four screws which fasten the Synthesizer Assembly to the bottom of the chassis. With the bottom cover removed, turn the unit over for access to the electrical connectors at the chassis bottom. Remove the Synthesizer cover. Check that line power is disconnected. Then lay the Synthesizer Assembly on the bottom of the chassis with some insulation to prevent shorts. Make electrical connections; the snap-on plugs for the shielded leads are labeled with plug number and the pin connectors for the colored-wire connections are labeled for wire color.

Figure 1.




INPUT GATE CONTROL
IC3
1820-0070
6 5 2 3 1 11 12
5 MHz
INPUT GATE
Q3,
Q2
5 MHz
INPUT
FROM
A13
BUFFER
AMPLIFIER
J3
IC1
1820-0322
PRESET DECADE
IC2
1820-0322
PRESET DECADE
IC5
1820-0322
PRESET DECADE
"1" "2" "4" "8"
5, 6
12
8
4 10 3 11 1
A1S1A
A1S1B
A1S1C

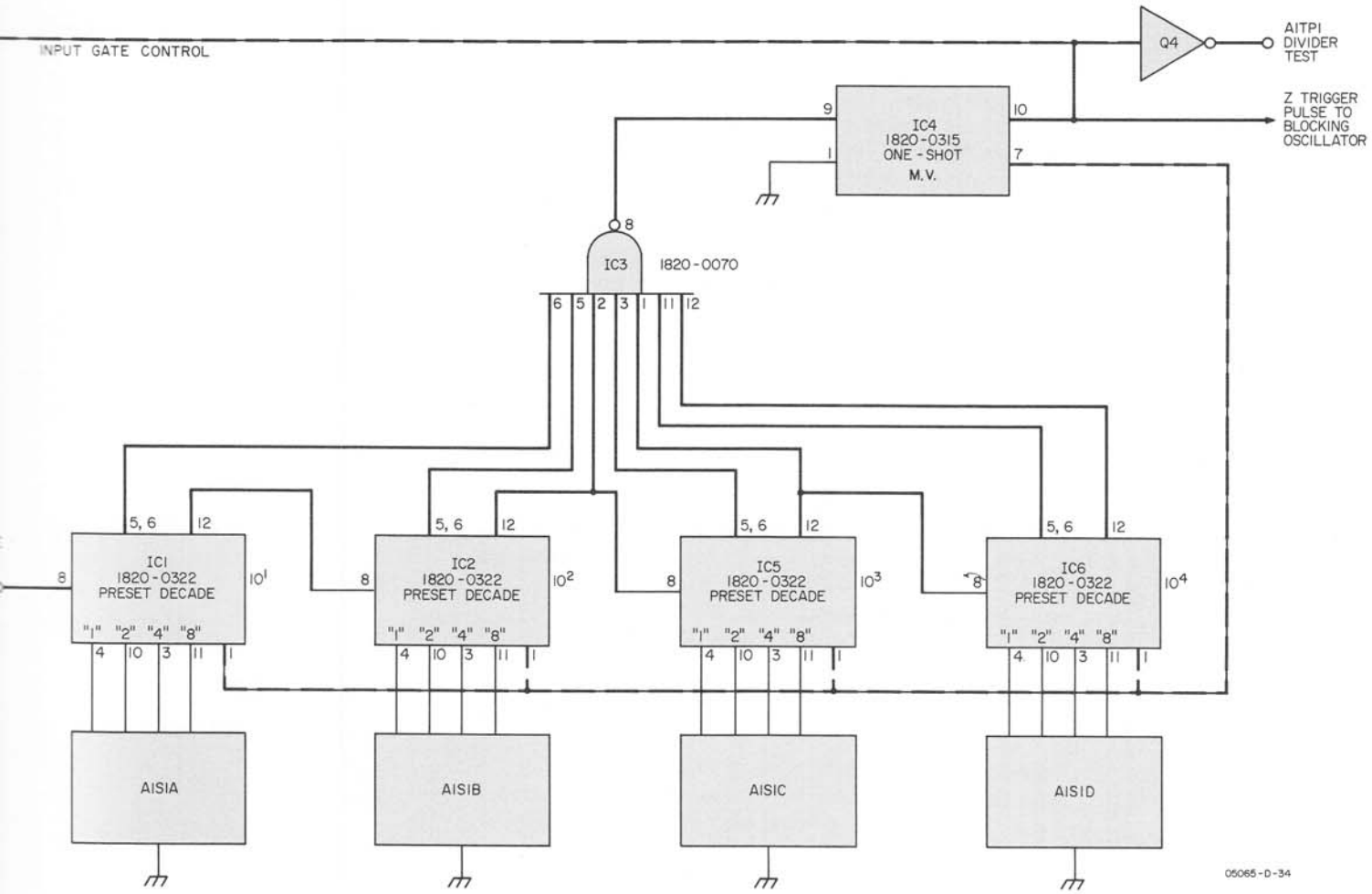


Figure 8-8. Synthesizer Assembly A1 Block Diagram
Digital Section

WARNING

WHEN THE CHASSIS BOTTOM IS EXPOSED, AVOID CONTACT WITH THE LINE TRANSFORMER TERMINALS AT THE REAR OF THE CHASSIS.

Faults may be isolated to the digital section or the phase-locked-oscillator section by using the table.

Connect a Period Counter to A1TP1 and adjust the thumbwheel switch as indicated in the table (Note original setting before changing thumbwheels). The output signal from the digital divider should have the period shown. If the period measurements are correct, set thumbwheel switch back to original setting and troubleshoot phase-locked-oscillator section. If periods are incorrect, then throubleshoot digital section. Note: If Y1 or associated components are suspected of failure see Paragraph entitled "A1Y1, A1L1, A1L2, A1L3, or A1L4 Check and Replacement."

MODULE REPLACEMENT

When Synthesizer Assembly A1 is replaced, the following adjustment is necessary:

a. Set TIME SCALE thumbwheel and HI/LO switches for the same settings as the replaced Synthesizer Assembly.

b. Set instrument to normal operation (CONTINUOUS OPERATION light on).

c. Set front panel OSC FREQ ADJ FINE control to 250.

d. Set CIRCUIT CHECK meter to CONTROL. Observing the meter indication, adjust OSC FREQ ADJ COARSE control for a zero reading.

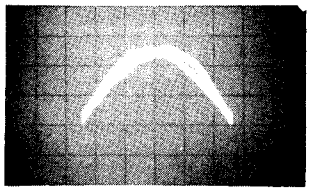
e. Set FUNCTION switch to LOOP OPEN.

f. Set OSC FREQ ADJ FINE control to 200.

g. Remove instrument top cover. Connect the vertical input of an oscilloscope to A8TP3 and the horizontal input to A8TP2.

h. Adjust oscilloscope for a pattern similar to the following waveform.

Optimized A8TP3 Output



Synthesizer A1TP1 Output Period (vs. Thumbwheel Switch Setting) Table

Time Scale Thumbwheel Setting	Signal Period at A1TP1 (μsec)
0000	2,000.0
0001	1,999.8
0002	1,999.6
0003	1,999.4
0004	1,999.2
0005	1,999.0
0006	1,998.8
0007	1,998.6
0008	1,998.4
0009	1,998.2
0010	1,998.0
0020	1,996.0
0030	1,994.0
0040	1,992.0
0050	1,990.0
0060	1,988.0
0070	1,986.0
0080	1,984.0
0090	1,982.0
0100	1,980.0
0200	1,960.0
0300	1,940.0
0400	1,920.0
0500	1,900.0
0600	1,880.0
0700	1,860.0
0800	1,840.0
0900	1,820.0
1000	1,800.0
2000	1,600.0
3000	1,400.0
4000	1,200.0
5000	1,000.0
6000	800.0
7000	600.0
8000	400.0
9000	200.0

i. Adjust A3R3 fully ccw. The oscilloscope pattern will disappear. Then adjust this control cw and as the pattern appears, adjust cw until the pattern just splits. Then back off slightly to where the pattern is similar to the optimized A8TP2 waveform.

j. Remove oscilloscope connections and replace top covers. Set OSC FREQ ADJ FINE to 250 and set FUNCTION switch to OPER.

k. Press LOGIC RESET pushbutton. CONTINUOUS OPERATION light will come on and stay on.

A1Y1, A1L1, A1L2, A1L3, or A1L4 CHECK AND REPLACEMENT

a. Set FUNCTION switch at LOOP OPEN.

b. Remove synthesizer assembly from instrument (see Troubleshooting). Remove module cover. Disconnect electrical power and turn the unit over. Using a piece of insulation to prevent shorts, reconnect the Synthesizer 5 MHz input to A1J2, the +20 volt lead (wht-red), to the appropriate jack and circuit board ground to chassis ground. Reconnect electrical power.

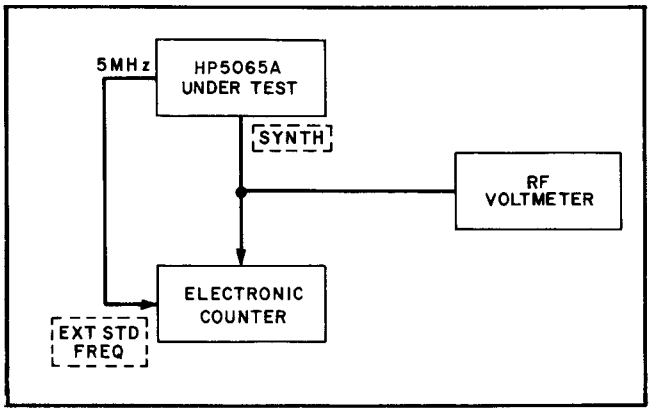
c. Remove Crystal Y1 and, using a high-impedance voltmeter, check voltage at junction of CR27 and R79. It should be 6 V ± 0.5 volts dc. If it is not, check bias circuitry: R71, R72, CR32, CR30, R73, Q23, CR27, etc. If there are no defective components, adjust R71 for the correct voltage.

d. Disconnect 5 MHz from A1J1 and replace Y1 in its socket.

e. Set TIME SCALE slide switch on synthesizer to LO.

f. Measure Synthesizer frequency at A1J3 using setup shown in the following illustration.

Figure 2.



g. If counter indication is greater than 5.314850 MHz or less than 5.314550 MHz, replace A1Y1 before proceeding.

h. Adjust L1 and L2 as necessary for a counter indication of 5.315700 ± 50 Hz.

i. Set TIME SCALE slide switch on Synthesizer to HI.

j. Adjust L4 as necessary for a counter indication of 5.315000 ± 50 Hz.

k. Set TIME SCALE slide switch on Synthesizer to LO. Check that counter indication is 5.314700 ± 50 Hz. If frequency is incorrect, repeat steps g through j.

l. When frequency at HI and LO settings are correct, turn off electrical power, disconnect the synthesizer, replace its cover, and then replace the Synthesizer in the 5065A unit.

m. Reconnect all Synthesizer electrical connections, apply electrical power.

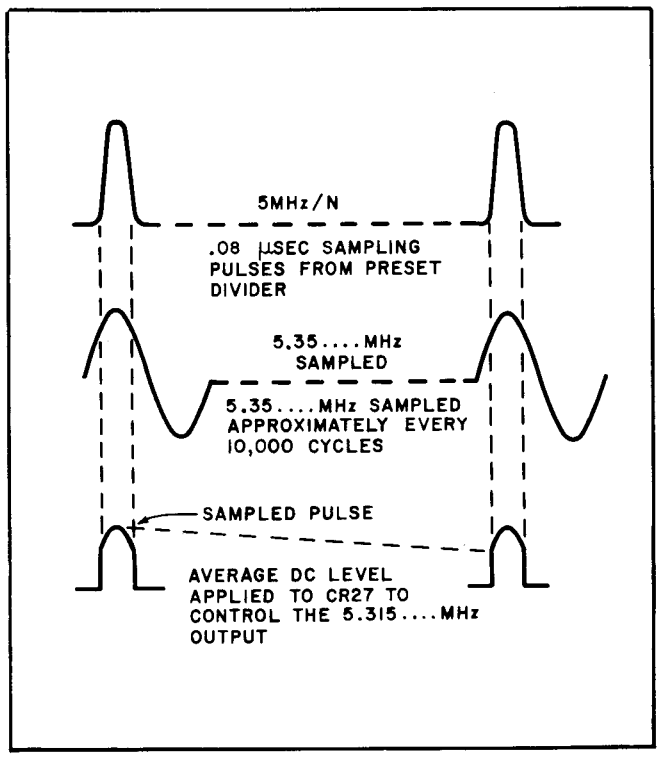
n. Connect the 5065A as shown in the following illustration and check Synthesizer output frequencies as described in the Performance Check for A1 Synthesizer.

PHASE LOCKED VOLTAGE CONTROLLED OSCILLATOR

The phase locked voltage controlled oscillator produces the 5.315...MHz signal applied (through A3 Multiplier) to the harmonic generator/step-recovery diode in A12 Assembly. In A12, 5.315...MHz is mixed with the 6.840...GHz phase-modulated signal (the 114th harmonic of 60 MHz). Oscillator frequency is determined by the bias voltage applied to varactor diode CR27.

The figure below illustrates the sampling process. The 5 MHz/n output pulse of the preset divider is the sampling pulse in the phase lock sampling circuit. The sampled output pulses of this circuit are integrated by the circuit time constant to a dc voltage representing a phase error. This dc voltage acts on CR27 to shift oscillator frequency for a zero dc output which corresponds to a phase-locked, "on frequency" condition.

Sampling Process



Prior to phase locking, the 5.315...MHz VCO (Q18 and associated components) oscillates at about 5.315...MHz, dependent on dc biasing by R71 and R72. Transistor Q21 buffers the oscillator and drives Q22 and Q26. The 5.315...MHz signal at T2 primary is the input signal for the sampler.

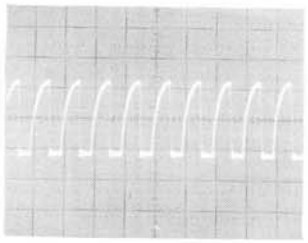
Transitors Q17, Q19, and associated components are a trigger circuit driven by output pulses from preset divider output gate IC5. This trigger circuit drives sampler blocking oscillator Q20. Transformer T1 receives 80 nsec pulses from Q20 at the 5 MHz/n frequency. These pulses "turn on" CR32 and CR33 each time they occur. The 5.315...MHz signal also present in T2 secondary is very close to the "mth" harmonic of 5 MHz/n. This "m" harmonic is sampled at the 5 MHz/n rate, filtered by L7 and C34, and applied to varactor diode CR27 to control oscillator frequency. Therefore, the voltage level at CR27 cathode determines oscillator frequency.

Buffer amplifier Q21 couples the Synthesizer frequency to tuned amplifier Q26, improving signal purity. This output connects to the front-panel SYNTHESIZER CHECK jack for test purposes and to A3 Multiplier Assembly for adding to the Multiplier 60 MHz signal.

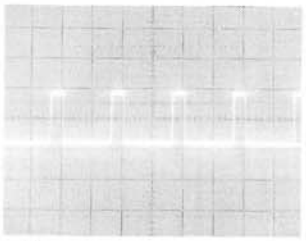
The 5.315...MHz VCO phase lock range is kept narrow to prevent phase locking to incorrect harmonics. To accommodate the dynamic range required to complete coverage of all UTC offset frequencies, the VCO has two overlapping frequency ranges, selected by HI/LO switch A1S2. Table 3-6 indicates the proper setting for synthesizer frequencies.

Oscillator output amplitude is stabilized by the rectified output from diodes CR34 and CR35. This output if filtered by C38 and C39. This AGC dc feedback connects to oscillator Q18 base.

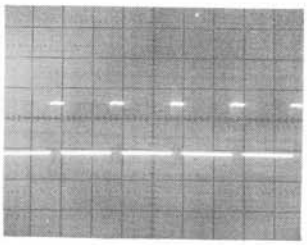
Transistor Q27 and associated components provide a Synthesizer failure signal to Logic Assembly A14. During normal Synthesizer operation, Q27 is biased off and no output signal results. If the Synthesizer loses phase lock, Q23 input becomes a random ac signal which can be observed at TP1. This signal is coupled through C37 and Q24 base, amplified in Q24, Q25, and rectified by CR36 and CR37. This rectified signal forward biases CR38 and turns Q27 on to send a signal to Logic Assembly A14. This turns off the CONTINUOUS OPERATION light. If blocking oscillator Q20 fails, a signal through CR39 will turn on Q27 and apply the same failure signal to the logic circuit.



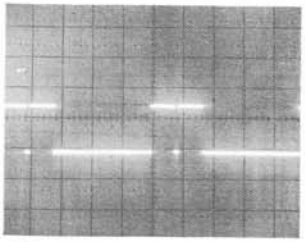
1 2 V/cm
.2 μsec/cm
dc coupled



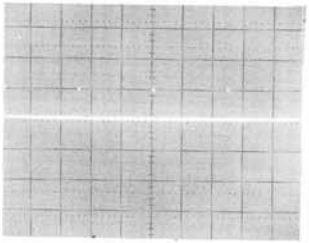
2 2 V/cm
1 μsec/cm
dc coupled



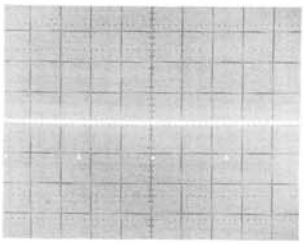
3 2 V/cm
10 μsec/cm
dc coupled



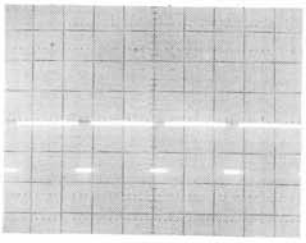
4 2 V/cm
50 μsec/cm
dc coupled



5 6 2 V/cm
.1 msec/cm
dc coupled



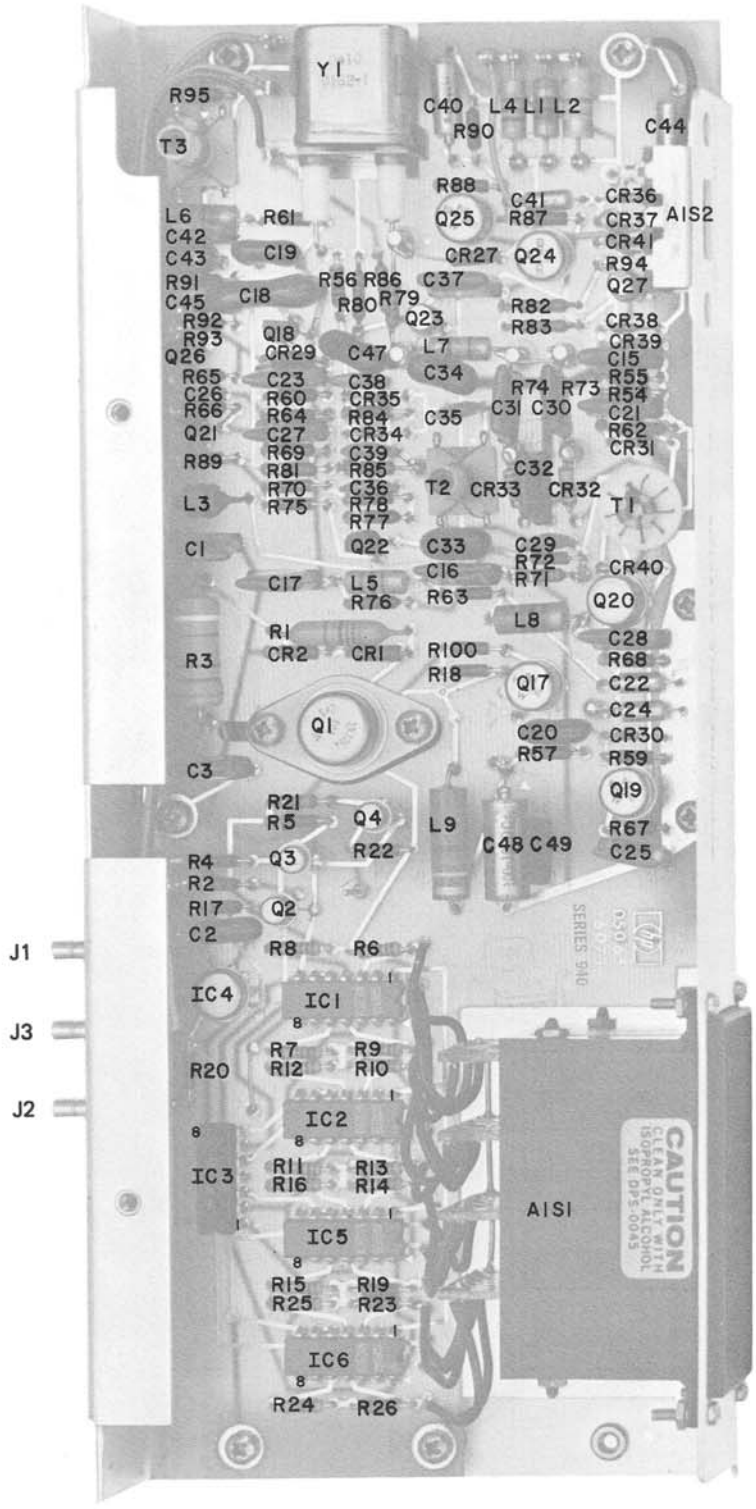
7 8 5 V/cm
.1 msec/cm
dc coupled

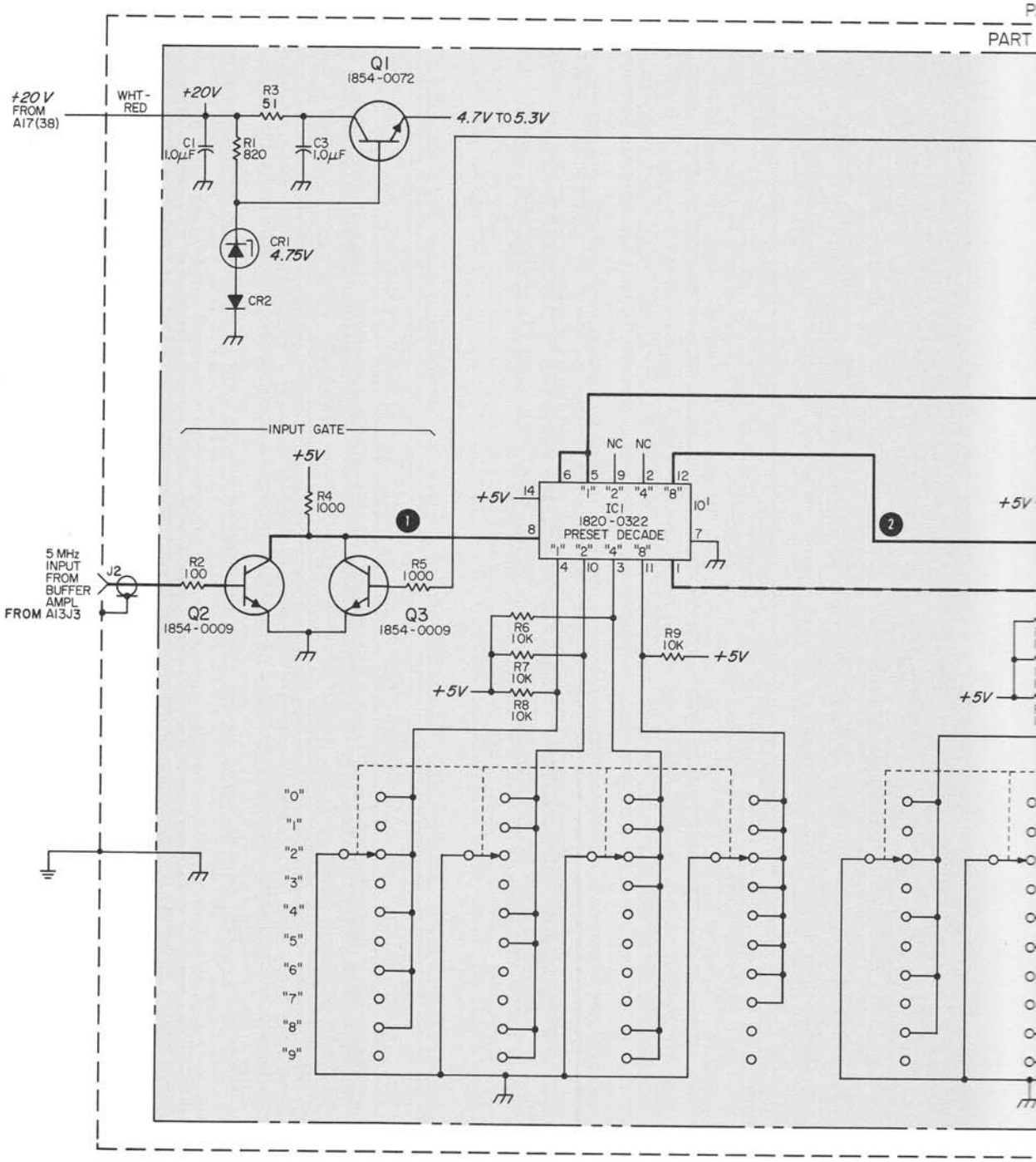


9 .2 V/cm
.1 msec/cm
dc coupled

Figure 8-9
SYNTHESIZER ASSEMBLY A1 DIGITAL SECTION
(Sheet 1 of 2)

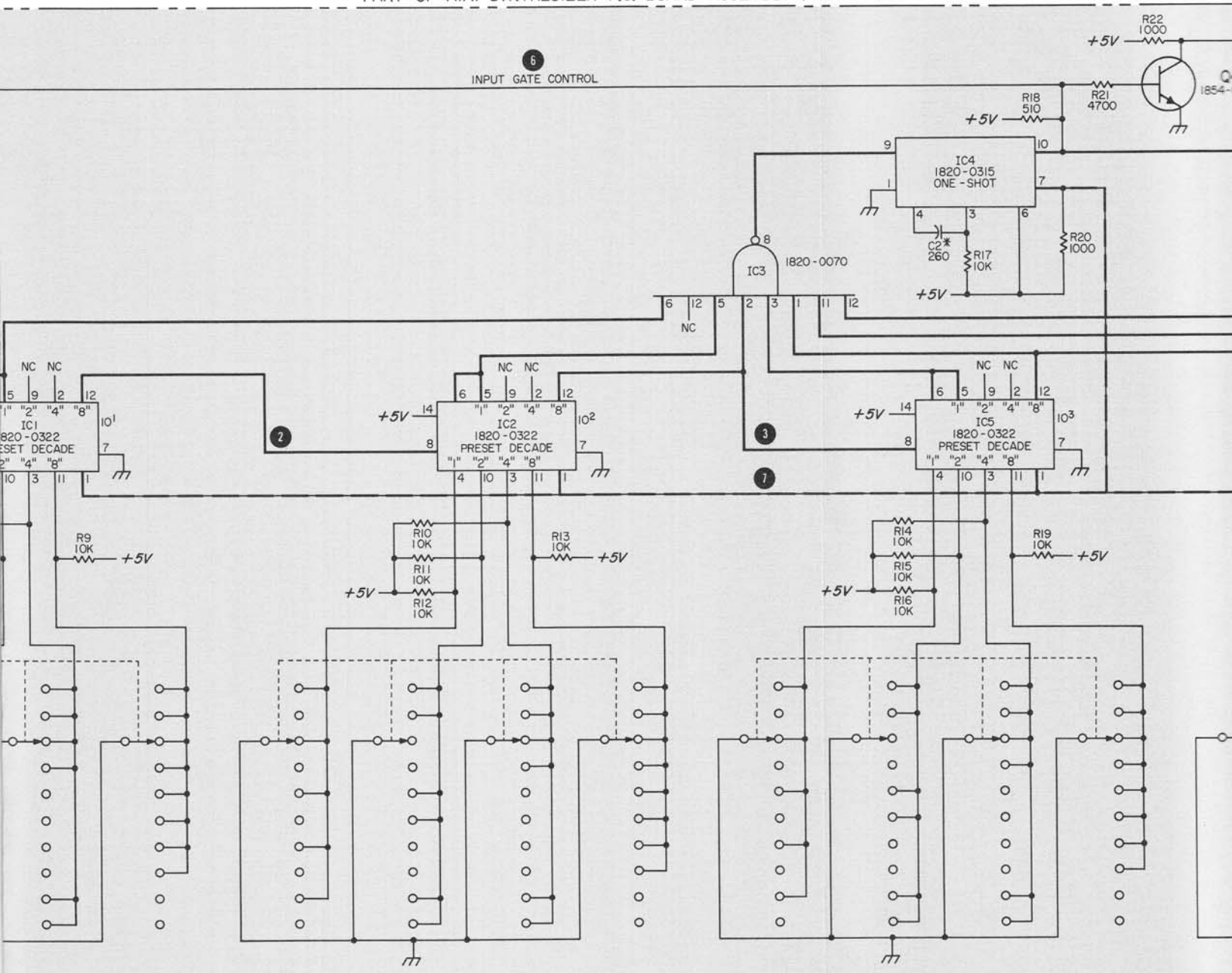
(See Page 8-17)


Y1
R95
T3
C40 L4 L1 L2
R90
C44
R88
C41
CR36
L6
R61
Q25
R87
CR37
AIS2
C42
CR41
C43
C19
CR27
Q24
R94
R91
R56 R86
C37
Q27
C45
C18
R80
R79
R82
R92
Q23
R83
CR38
R93
Q18
L7
CR39
Q26
CR29
C47
C15
R65
C23
C38
C34
R74 R73
R55
C26
R60
CR35
R54
R66
R64
R84
C35
C31 C30
C21
Q21
C27
CR34
R62
R69
C39
CR31
R89
R81
R85
C32
L3
R70
C36
T2
CR33
CR32
T1
R75
R78
R77
C1
Q22
C33
C29
R72
C16
CR40
C17
L5
R71
R76
R63
Q20
L8
R1
C28
R3
CR2
CR1
R100
R68
R18
Q17
C22
C24
Q1
C20
CR30
R57
R59
C3
Q19
R21
R5
Q4
L9
R67
C48 C49
C25
R4
Q3
R22
R2
R17
Q2
C2
J1
R8
R6
IC4
IC1
J3
R7
R9
R20
R12
R10
J2
IC2
IC3
R11
R13
R16
R14
AIS1
IC5
R15
R19
R25
R23
IC6
R24
R26
CAUTION
CLEAN ONLY WITH ISOPROPYL ALCOHOL
SEE DPS-0043
SERIES 940


PART
+20V FROM A17(38)
WHT-RED
+20V
R3 51
Q1 1854-0072
4.7V TO 5.3V
C1 1.0μF
R1 820
C3 1.0μF
CR1 4.75V
CR2
INPUT GATE
+5V
R4 1000
5 MHz INPUT FROM BUFFER AMPL FROM A13J3
J2
R2 100
R5 1000
Q2 1854-0009
Q3 1854-0009
NC NC
IC1 1820-0322 PRESET DECADE
"1" "2" "4" "8"
R6 10K
R7 10K
R8 10K
R9 10K
"0"
"1"
"2"
"3"
"4"
"5"
"6"
"7"
"8"
"9"

PART OF A1 SYNTHESIZER ASSEMBLY (05065-6076) (NOTE 1) SERIES 1908

PART OF A1A1 SYNTHESIZER P.C. BOARD ASSEMBLY (05065-6073) SERIES 1908



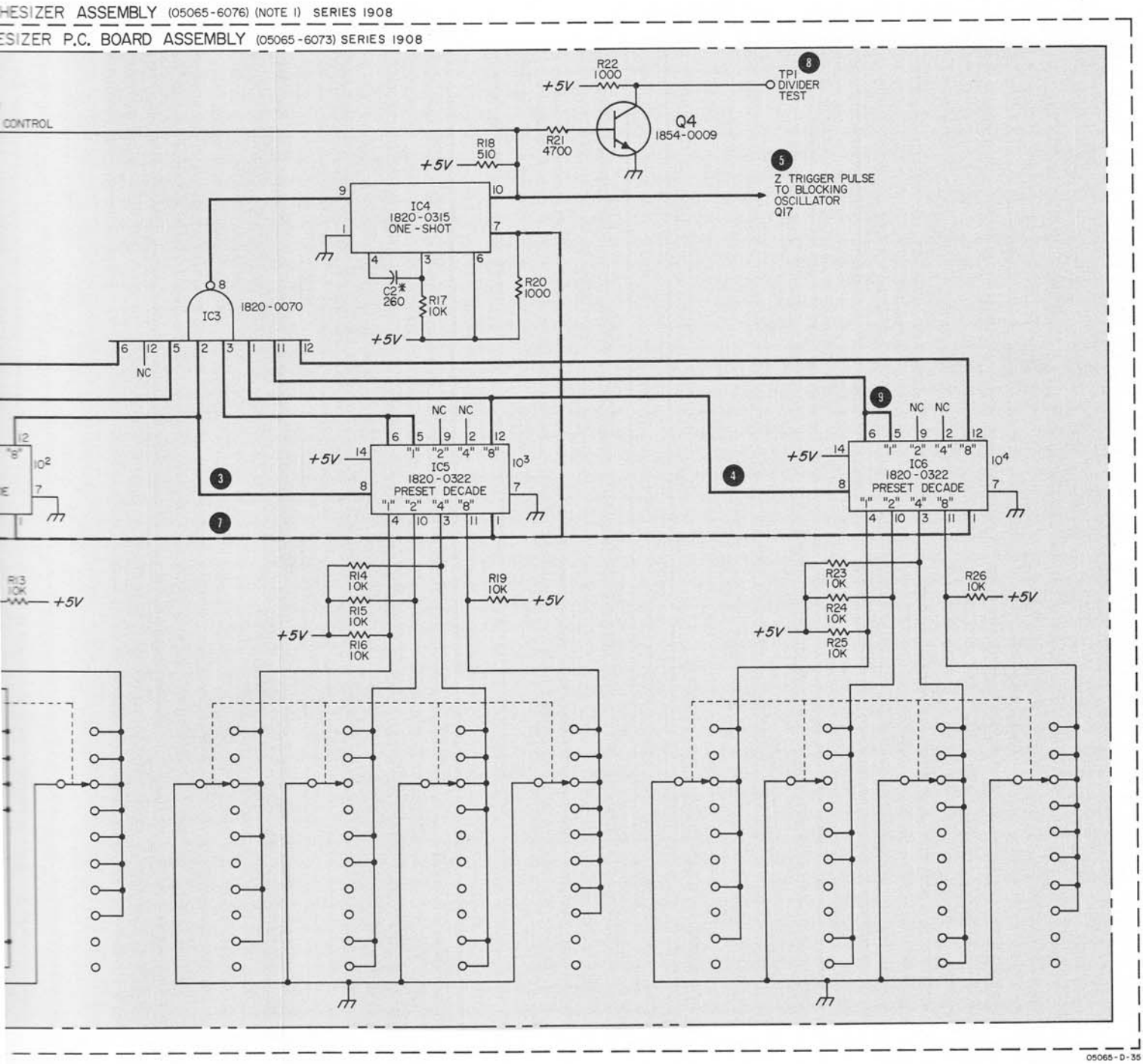
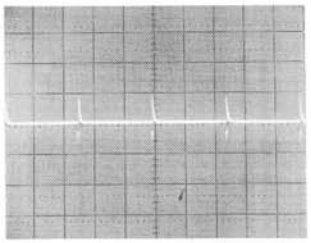


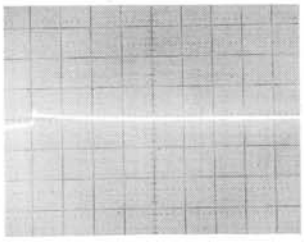
Figure 8-9. Synthesizer Assembly A1 Digital Section
(Sheet 1 of 2)

Figure 8-9
SYNTHESIZER ASSEMBLY A1 PHASE-LOCKED OSCILLATOR SECTION (Sheet 2 of 2)

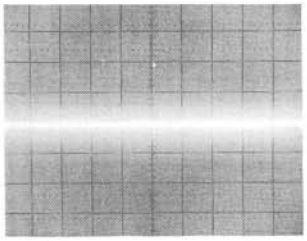
(See Page 8-19)



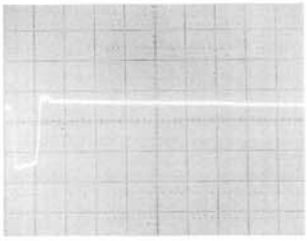
⑩ .1 V/cm
.1 msec/cm
dc coupled



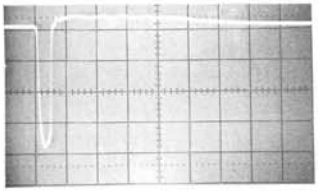
⑩ .2 V/cm
1 μsec/cm
dc coupled
(Puse width)



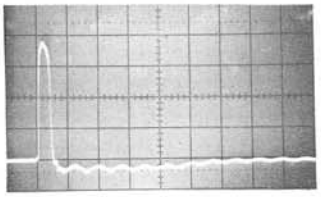
⑪ 1 V/cm
50 μsec/cm
ac coupled



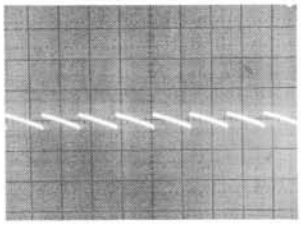
⑪ 1 V/cm
.1 μsec/cm
ac coupled
(Pulse width)



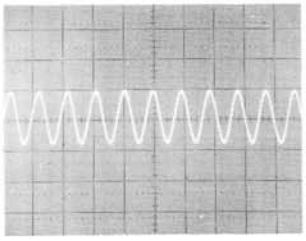
⑫ .5 V/cm
.2 msec/cm
ac coupled



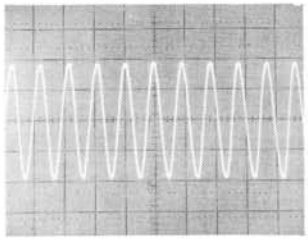
⑬ .2 V/cm
.1 μsec/cm
dc coupled



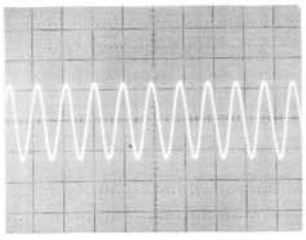
⑭ .05 V/cm
.2 msec/cm
dc coupled



⑮ .05 V/cm
.2 μsec/cm
ac coupled



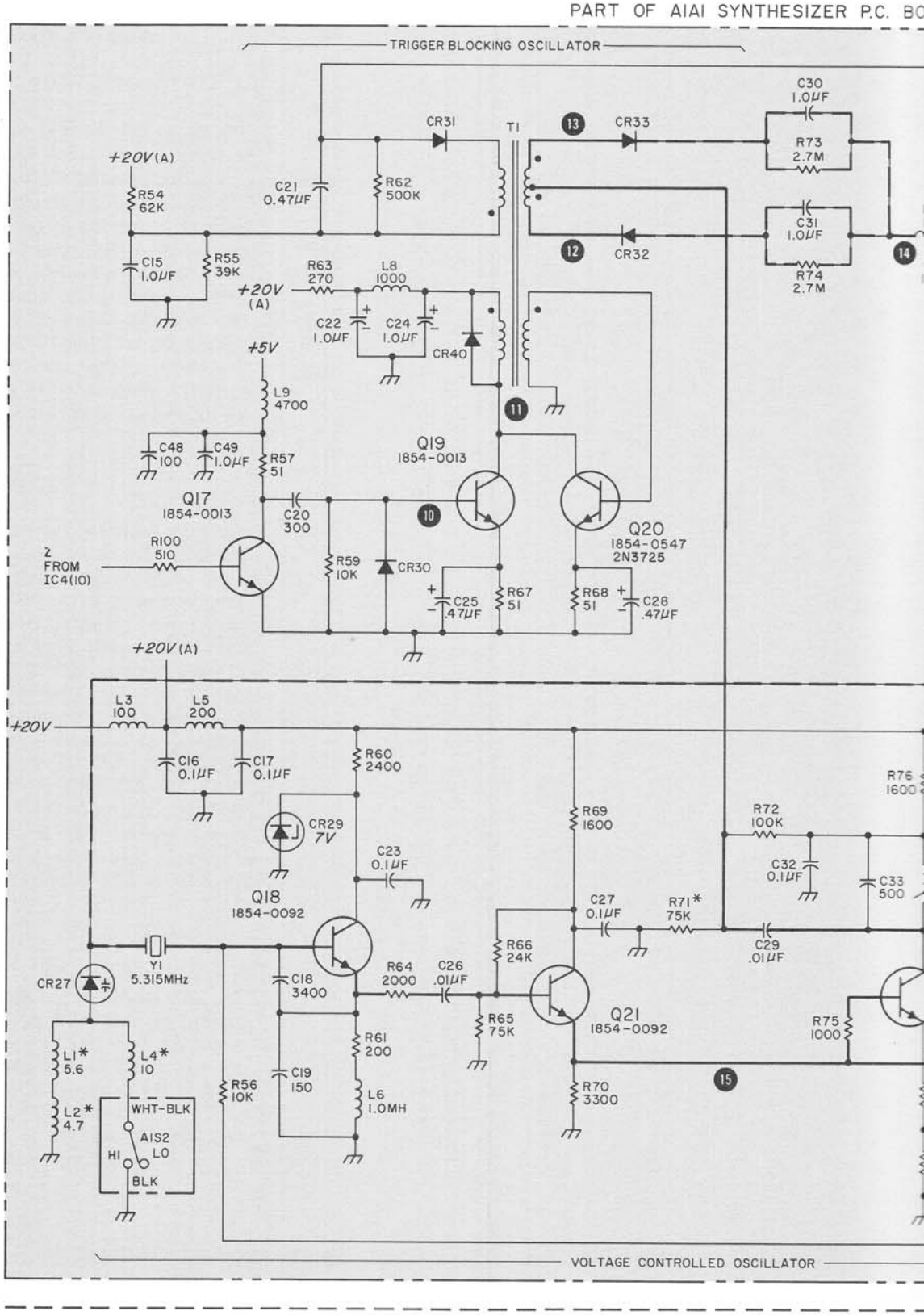
⑯ 1 V/cm
.2 msec/cm
ac coupled



⑰ .05 V/cm
.2 μsec/cm
ac coupled

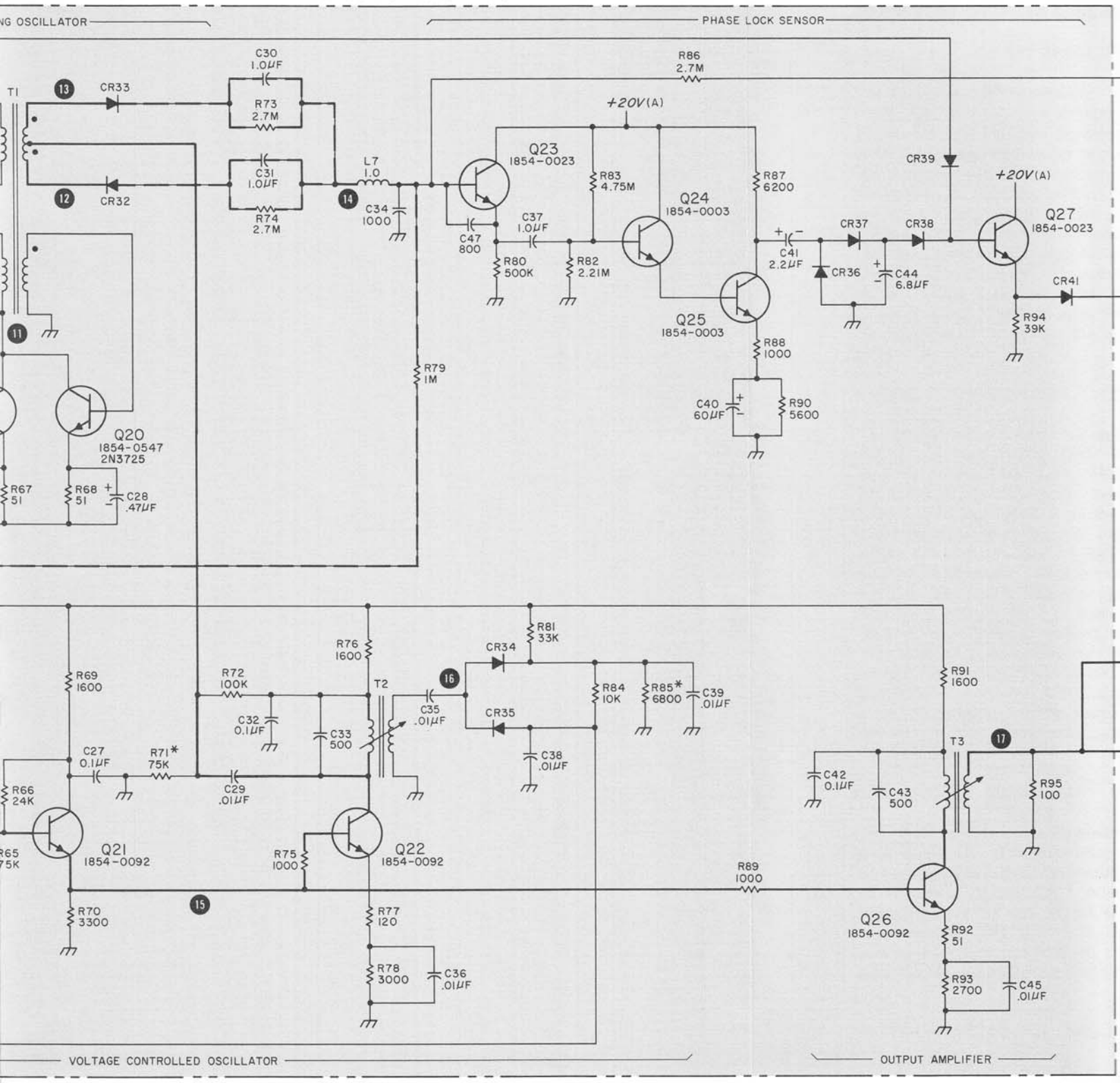
PART OF A1 SYNTHESIZER ASSE

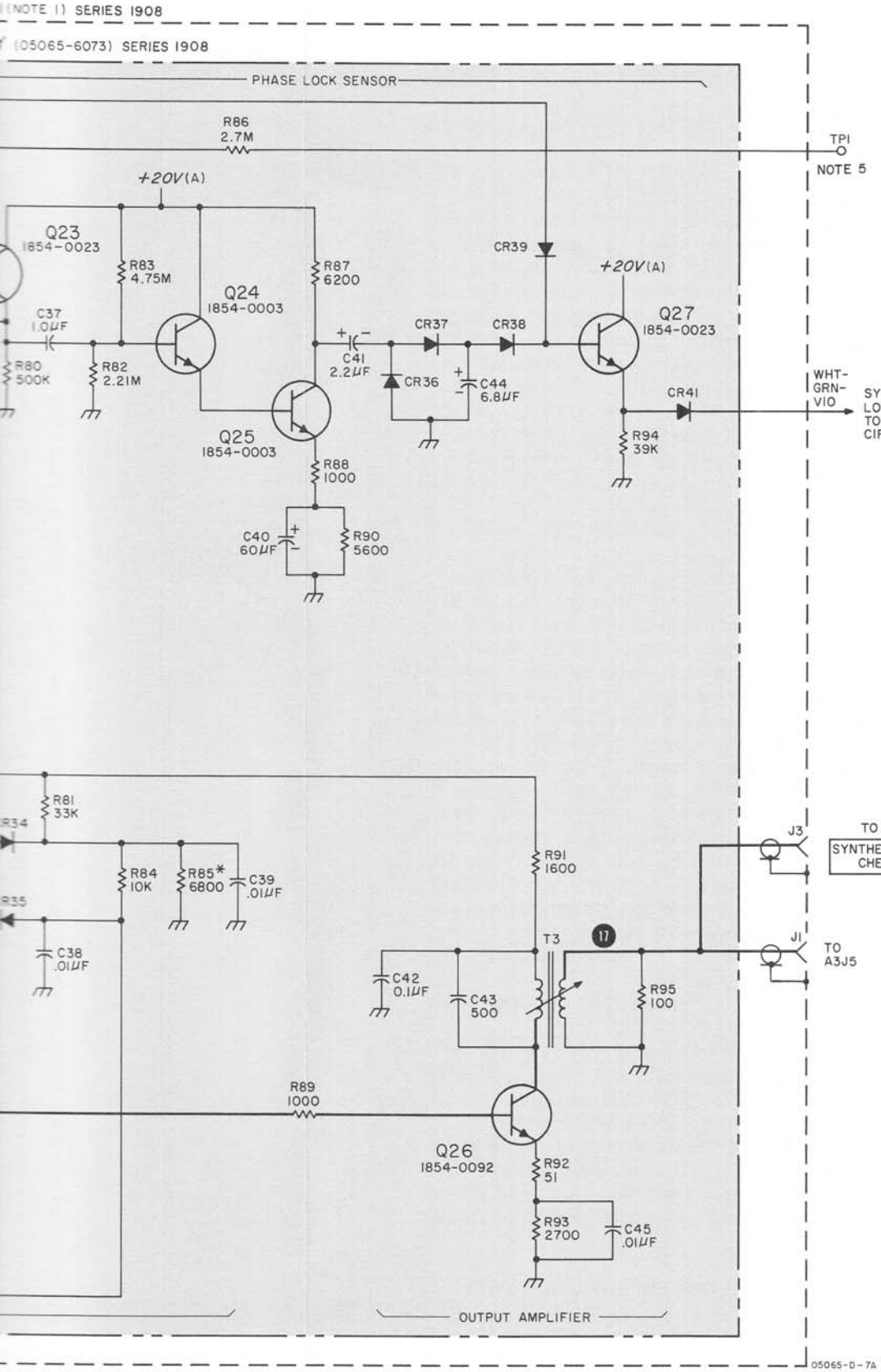
PART OF A1A1 SYNTHESIZER P.C. BO



PART OF A1 SYNTHESIZER ASSEMBLY (05065-6076) (NOTE 1) SERIES 1908

PART OF A1A1 SYNTHESIZER P.C. BOARD ASSEMBLY (05065-6073) SERIES 1908





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS; INDUCTANCE IN MICROHENRIES
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN.
4. SEE THUMBWHEEL SWITCH PAGE 8-10
5. TP1 BECOMES A RANDOM AC SIGNAL WHEN SYNTHESIZER IS OUT OF LOCK.

REFERENCE DESIGNATIONS

NO PREFIX	A1	A1A1
		C1-3,15-45, 47-49 CR1,2,27, 29-39,41 IC1-6
	J1-3	L1-9 Q1-4,17-27 R1-26, 54-57, 59-95,100
	S1,2	T1-3
TP1		TP1 Y1

Figure 8-9. Synthesizer Assembly A1 Phase-Locked Oscillator Section (Sheet 2 of 2)

A2 BATTERY CHARGER ASSEMBLY THEORY

CHARGING CURRENT REGULATOR CIRCUIT

The charging current regulator is made up of A2CR7, A2Q5, Q6, and Q4. Ac voltage from T1 is applied to A2(10, 11) and rectified by bridge network A2CR1 to A2CR4. Voltage regulation occurs through A2Q5 and Q4. A2Q6 monitors battery charging current by sensing the voltage drop across A2R12 and A2R13. Increases in battery charging current are sensed by A2Q6 which conducts and increases voltage drop across A2R7. The decrease in bias at A2Q5 base regulates the charging current from Q4 to within limits set by A2CR7. In the FLOAT position of S6, the battery receives a trickle-charge. When S6 is in FAST position A2R12 is bypassed which increases the charging current to the battery.

BATTERY LAMP CONTROL CIRCUIT

The battery lamp control circuit is comprised of A2Q1, Q2, Q3, Q4, and A2CR6, CR8. In the FLOAT position, BATTERY lamp DS3 is off. Multivibrator A2Q1, Q3 is off and A2Q2 is biased off. When the ac line is interrupted, a voltage signal from the Battery Cut-in Circuit turns on A2Q7 and Q2, and triggers the multivibrator A2Q1, Q3. This causes the BATTERY lamp to flash on and off. Operating voltage comes from the battery through Q14 to the Power Supply and Regulator A15. The lamp will continue to flash until the ac power is restored and RESET is pressed. In RESET position CR8 gate element is grounded turning CR8, Q2, the multivibrator circuit, and the lamp off. In the FAST CHARGE position S6 shorts out A2R12 and increases the battery charging current. Another section of S6 also provides a ground for the battery lamp through A2R6 to turn the lamp on continously.

BATTERY CUT-IN CIRCUIT

The battery cut-in circuit is made up of A2CR9, Q8, Q9, Q12, and Q15. The dc voltage from the instrument power supply is monitored through CR9. As long as the dc voltage is present Q8 conducts and Q9 is cut off. When ac power is interrupted, Q8 is turned off and Q9 is turned on. This turns Q12, Q15, and Q13 on. This action also turns on the dc power switch Q14 and sustains instrument operation from the battery.

BATTERY DISCONNECT CIRCUIT

The Battery Disconnect Circuit consists of A2CR11, Q10, Q11, K1, and CR15. During battery operation, battery voltage monitored through CR11 keeps Q10 turned on. When the battery voltage decreases to approximately 23 volts, Q10 turns off and causes Q11 to turn on. This in turn energizes differential relay K1, and disconnects the battery. When ac power is reapplied, Q10 again conducts. This reverses the polarity of A2K1 and reconnects the battery.

OPERATIONAL CHECK

a. Observe the CIRCUIT CHECK BATTERY position; indication should be between 30 and 50.

b. Disconnect ac cord from ac line; BATTERY lamp should flash on and off. RESET has no effect.

c. Connect ac power cord to ac line. RESET BATTERY switch; BATTERY lamp should stop flashing. Set BATTERY switch to FAST CHARGE; BATTERY lamp should light. Return switch to FLOAT position and BATTERY lamp will go out. This completes the check.

TROUBLESHOOTING

NOTE

These tests check individual circuits on Battery Charger Assembly A2. If failure is indicated in a circuit, repair the circuit and perform battery charger operational check.

a. Charging Current Regulator.

1. Charging current to the battery should be:

FLOAT: 12 to 34 mA (see Paragraph 5-35)
FAST CHARGE: 90 to 150 mA (see Paragraph 5-35)

2. If the current differs substantially check A2CR1 to CR4 for power rectification and CR7 for indicated voltage. Check Q4, A2Q5, A2Q6 operation. Check S6.

b. Battery Lamp Control.

1. If the lamp does not flash when ac is interrupted, check Q1, Q3 multivibrator, and check that collector of A2Q2 is below 1 volt.

2. If the lamp does not light with switch S6 in FAST CHARGE check S6 and DS3 or R6.

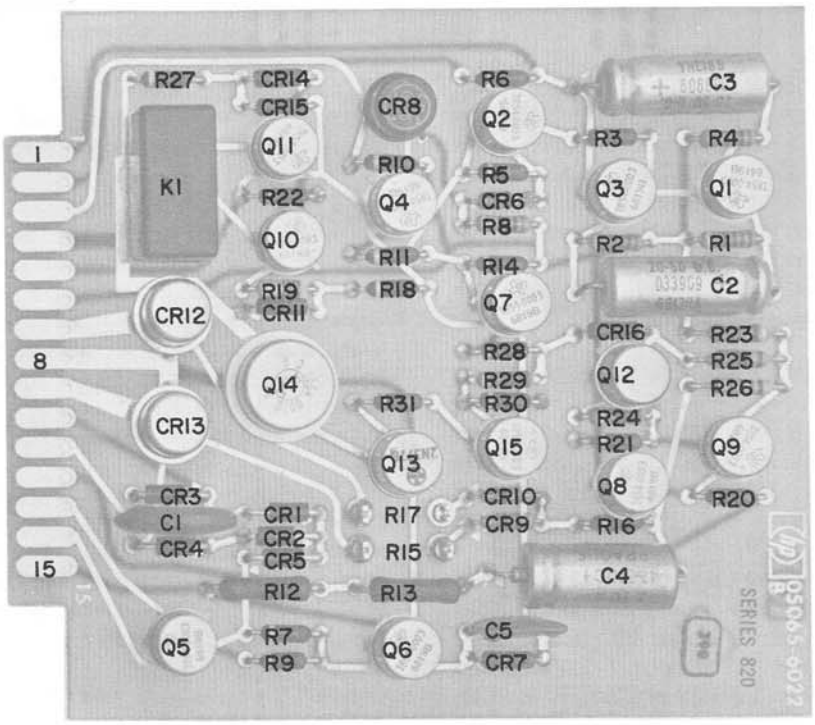
3. If Battery lamp won't light, check lamp DS3 and S6. If it won't go out, manually ground the + gate element of CR8. If the lamp goes out, check S6, otherwise, check CR8, Q2, Q1, and Q3.

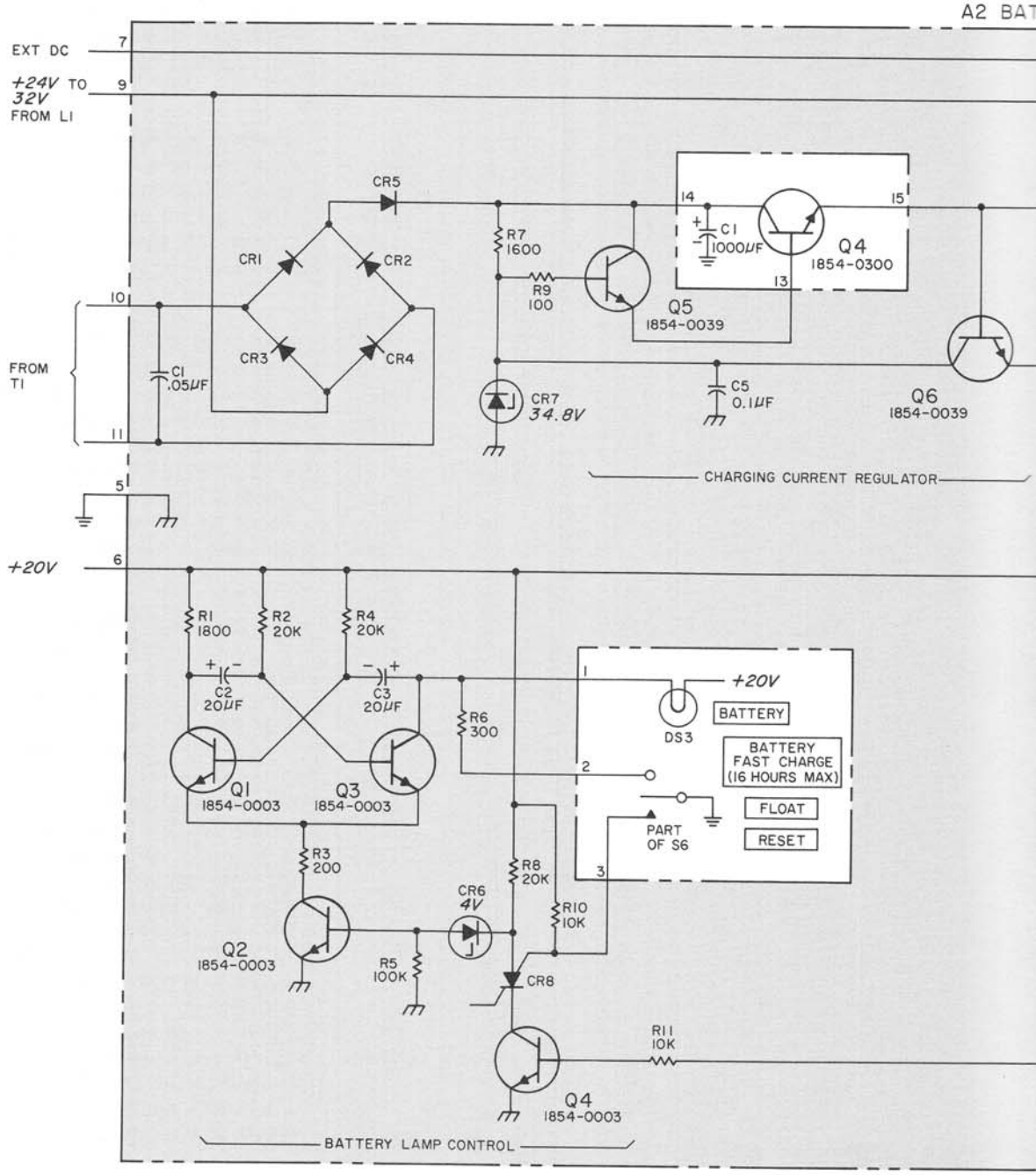
c. Battery Cut-in Circuit.

1. Disconnect ac power cord from ac power source. Instrument should switch to Battery Operation and DS3 should flash on and off. If this does not occur, check that collector A2Q12 increases from approximately 10 volts to 20 volts. If not check Zener voltages of A2CR9 and replace if it is outside the 10 to 12 volt range. Replace A2Q8, 9 and 12 successively in that order.

Figure 8-10
A2 BATTERY CHARGE ASSEMBLY (OTPION 002 AND 003)

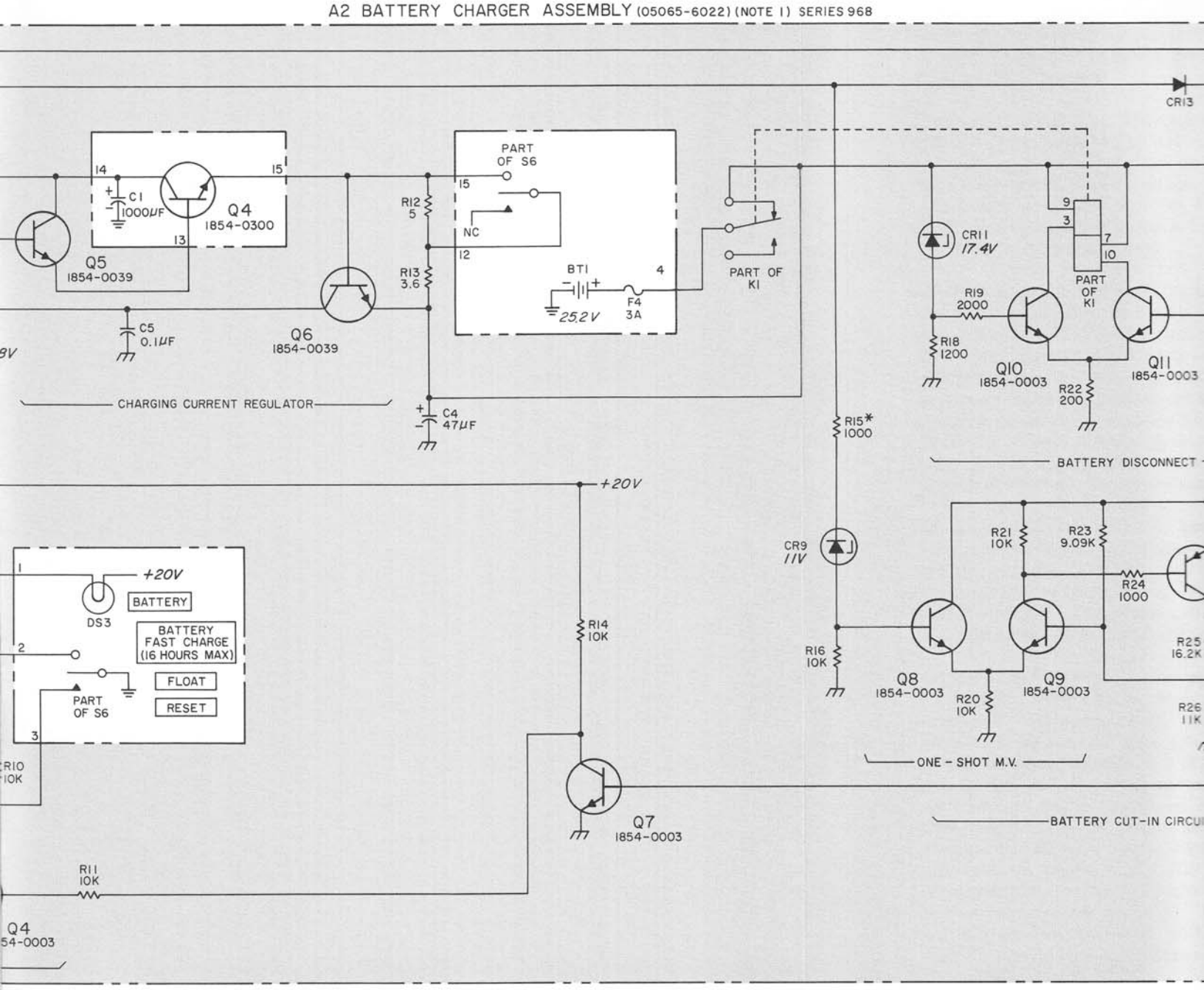
(See Page 8-21)


R27
CR14
CR15
CR8
R6
Q2
C3
R3
R4
1
K1
Q11
R10
R5
Q4
CR6
R8
Q3
Q1
R22
Q10
R11
R14
R2
R1
R19
R18
Q7
C2
CR12
CR11
CR16
R23
8
R28
R25
Q14
R29
Q12
R26
R31
R30
CR13
R24
R21
Q15
Q9
Q13
Q8
CR3
CR10
R20
C1
CR1
R17
CR9
R16
CR4
CR2
R15
CR5
15
C4
R12
R13
Q5
R7
Q6
C5
R9
CR7
SERIES 820
05065-6022



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN

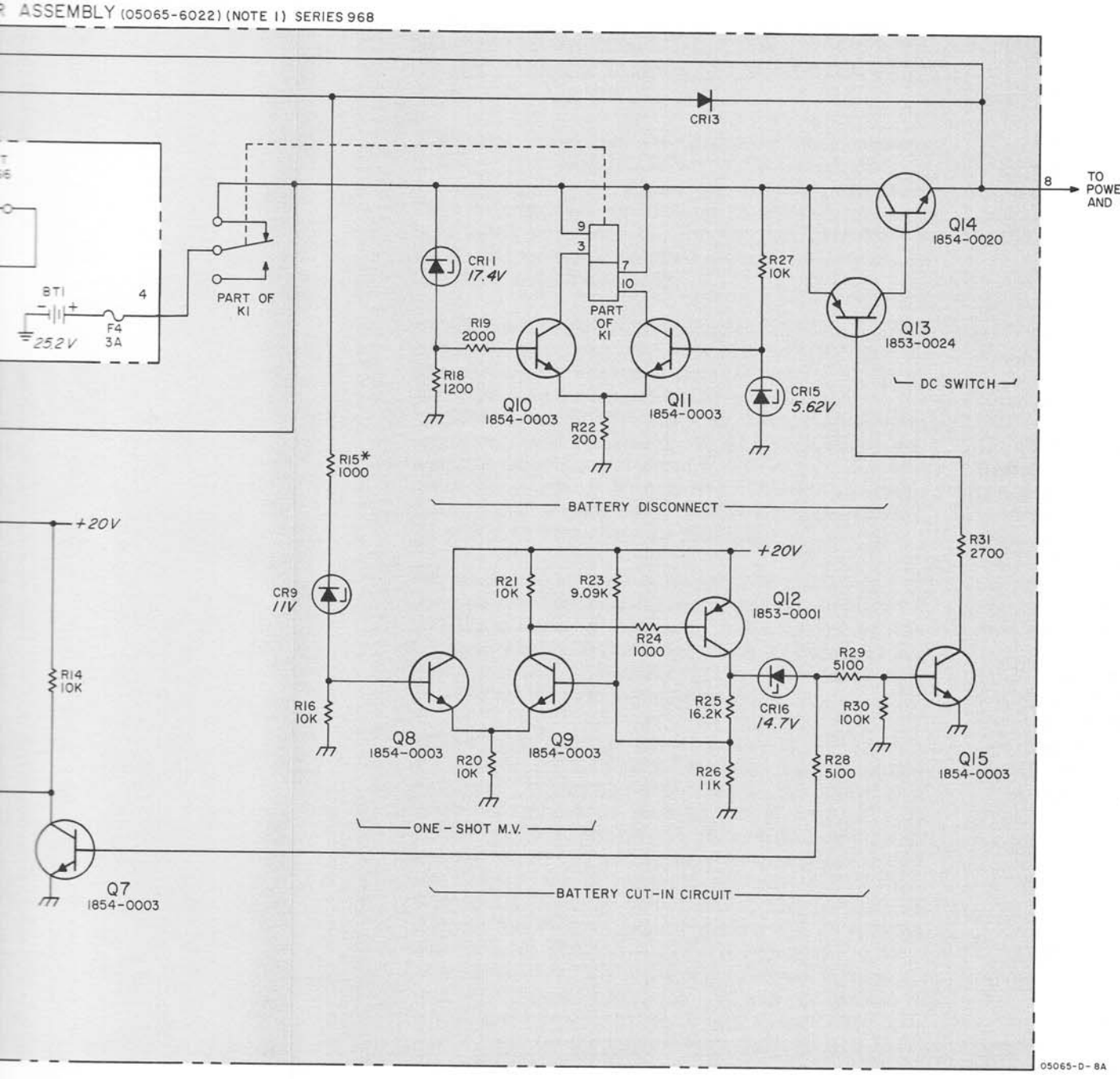


REFERENCE DESIGNATIONS

NO PREFIX	A2
BT1	
C4	C1-5 CR1-16
DS3	
F4	
	K1
Q4	Q1-15
	R1-31
S6	S1

DELETED:
CR12, 14
CR10, R17

Figure 8-10.



EFERENCE DESIGNATIONS

NO PREFIX	A2
BT1 C4	C1-5 CR1-16
DS3 F4	K1
Q4	Q1-15
R6	R1-31
	S1

DELETED:
CR12, 14
CR10, R17

Figure 8-10. A2 Battery Charge Assembly (Option 002 and 003)

60 MHz FREQUENCY MULTIPLIER A3 THEORY

Frequency Multiplier A3 provides a stable, spectrally clean, 300 milliwatt, 60 MHz signal which connects to harmonic generator/step recovery diode in A12 RVFR Assembly. Another output is the isolated 5 MHz signal to A13 Buffer Amplifier.

The 5 MHz signal from A10 Quartz Oscillator connects through input jack J2 to Q1 buffer amplifier; then through an isolating network to first multiplier stage Q2. Q1 output couples through T1 and through J3 to A13 Buffer Amplifier. R8, R9, R10, and R12 form a 10-dB pad to prevent feedback from Q2 to A10 Quartz Oscillator and output circuits.

Q2 modulator doubler stage doubles 5 MHz to 10 MHz and phase modulates the 5 MHz input at a 137 Hz rate. The primary in Q2 collector circuit is tuned to 5 MHz by C19 producing a strong 10 MHz second harmonic in the rectified output of CR1 and CR2. Phase Modulation is accomplished by varactor diodes CR3 through CR6. Varactor capacitance is varied at 137 Hz by the modulation signal from J1 through R11. This 137 Hz modulation signal is generated in the modulation oscillator portion of A8 Phase Detector Assembly.

Q6 doubles 10 MHz with CR7 and CR8 producing a 20 MHz second harmonic full-wave rectified output. T3 primary is tuned to 10 MHz by C30. Q8 triples with squaring diodes CR11 through CR14 producing strong odd harmonics. C49 tunes L20 to the input 20 MHz and C52 tunes L24 to the 60 MHz output.

Q3 is a MOS FET which furnishes high input impedance for isolation between Q8 tripler stage and the output amplifiers. Q3 voltage gain is about 20. Class A rf amplifiers Q5 and Q7 drive Q9 output amplifier. Q9 output connects through a 3-dB pad (C53, R38, R39, and R41) to J8. J8 output connects through J7 to TP1 and through the pi matching network of C61, C57, C59, and L25 to J4 output jack. This pi network matches the 50 ohm output impedance at J8 with the step-recovery diode in A12 RVFR Assembly. 5.315... MHz connects to the pi matching network through J5 from A1 Synthesizer Assembly. R3 sets the amount of 5.315...MHz that adds to the 60 MHz output. R40 controls dc bias for the step-recovery diode in A12 RVFR Assembly.

Voltage divider R28 and R34 biases feedback diodes CR9 and CR10. These diodes rectifiy the 60 MHz output and produce a dc feedback signal to control Q3 bias with feedback amplifier Q4. In this manner, the 60 MHz output is amplitude stabilized.

A3 MAINTENANCE

NORMAL OPERATION

a. J4 output is 60 MHz, phase modulated at 137 Hz, plus 5.315...MHz that comes from the A1 Synthesizer Assembly.

b. J3 output is 5 MHz, 1 volt into 50 ohms.

c. TP2 is the AGC voltage test point. When Multiplier is operating normally, this voltage will be 4.5 Vdc or greater.

OPERATIONAL CHECK

a. Measure dc AGC voltage at TP2; should be 4.5 V or greater. If less, complete loop alignment procedure, including realignment of the Multiplier pi matching network of Section 5-19, LOOP ALIGNMENT PROCEDURE.

b. Remove the short cable connecting to J8. Using the Micon-to-BNC test cable provided, connect a 50-ohm coaxial load to J8. Connect an RF Voltmeter to this load. The RF meter should read 2.7 to 3.0 V rms. Excessive voltage at this point means that the AGC circuit is not functioning properly.

c. Reconnect P8 and disconnect cable from J4. Connect the test cable with 50-ohm load to J4 and connect the RF voltmeter to the 50-ohm load. The voltmeter should indicate the presence of 60 MHz. Generally this signal will be 1 volt or greater. However, this voltage level will vary a great deal from unit to unit depending on the tuning of the pi matching network in the A3 Multiplier. Reconnect the 60 MHz output cable to A3J4.

d. Remove the cable from J2. This removes the 5 MHz input from A3 leaving only the 5.315...MHz signal on output jack J4. The RF voltmeter should read about 20 mV (this voltage depends on the setting of R3). As a further check, R3 may be adjusted and the change in voltage noted.

NOTE

R3 should be returned to its original setting.

e. Remove the P5 connector. This removes the 5.315...MHz signal. The output voltage should drop to near zero. Replace connections to J5 and J2.

f. Remove cable from J3. Connect test cable and 50-ohm load to J3. Connect RF voltmeter to 50-ohm load. RF voltmeter should read approximately 1 V rms.

g. Remove RF voltmeter and test cable. Reconnect cable to J3. This completes the test. If output signal levels measured above are correct, but there does not appear to be any RF excitation on the A12 RVFR Assembly, the A3 Assembly should be realigned per LOOP ALIGNMENT PROCEDURE, Section 5-19.

TROUBLESHOOTING AND REPAIR

a. REALIGNMENT AFTER REPAIR. When repairs are made within the A3 Assembly, the repaired circuit must be retuned. The following paragraphs give

alignment procedures for the various sections. A 50 MHz oscilloscope, an RF voltmeter, a 50-ohm coaxial load, and the Micon-to-BNC test cable provided are required for these adjustments. After initial alignment and the A3 Assembly reinstalled, the instrument should be completely readjusted as described in LOOP ALIGNMENT PROCEDURE, Section 5-19.

b. ALIGNMENT OF BUFFER AMPLIFIER STAGE Q1.

1) Remove cable from J3. Connect a 50-ohm coaxial load to J3 using the test cable provided and connect RF voltmeter to the 50-ohm load.

2) Remove shield cover for access to C1, C19, C30, and C49.

2) Adjust C1 for maximum signal at the voltmeter. There should be two signal peak for a complete rotation of C1. Tune for the highest peak.

4) Remove voltmeter and test cable from J3 and reconnect P3 to this jack.

c. ALIGNMENT OF DOUBLER STAGES Q2 and Q6.

1) Connect oscilloscope to drain of Q6 and adjust C19 to tune Q2 doubling stage. Select the higher of the two peaks observed.

2) Connect the oscilloscope to the drain of Q8 and adjust C30 to tune Q6 doubling stage. Select the higher of the two peaks observed.

3) Ground TP1 to prevent feedback. Then, using the test cable provided, remove the cable from J8 and connect a 50-ohm load to this jack. Connect the oscilloscope to the 50-ohm load.

4) Adjust C49 for maximum scope signal. Remove the test cable and reconnect P8 to J8.

5) Readjust C19 and then C30 as described in steps 1 and 2. C19 and C30 adjustment is now complete.

d. ALIGNMENT OF Q8 TRIPLER STAGE AND FINAL AMPLIFIER STAGES.

1) Ground TP2 to prevent feedback so that voltages may be monitored within the AGC loop.

2) Remove jumper cable from J8 and use the test cable provided to connect a 50-ohm coaxial load. Connect an RF voltmeter to the 50-ohm load.

3) Sequence through the following adjustments, each time monitoring the drain (or collector) of the following stage with an oscilloscope. In the case of the last stage, Q9, use the RF voltmeter indication for tuning. Starting with C49, retune each of these adjustments at least once:

C18, C33, C46, C49, C52

4) Put the cover on the A3 Assembly and retune C52, C18, C33, and C46 for a maximum indication on the RF voltmeter. Note the voltmeter reading. It should be between 3.2 and 3.6 volts.

5) Remove short from TP2. Voltmeter reading should drop to 2.7 to 3.0 volts due to the AGC feedback. Connect a dc voltmeter to TP2. With the preceeding multiplier adjustments optimized, this AGC voltage should be about 4.5 volts.

6) Remove the test cable and reconnect the jumper cable to J8.

e. A3 MATCHING NETWORK ADJUSTMENTS

The matching network adjustments are as follows:

R40 ..... This control sets bias for the step-recovery diode in the A12 Assembly.

C59, C61, and L25 ..... These adjustments match the multiplier output to the load presented by the step-recovery diode circuit in the A12 Assembly.

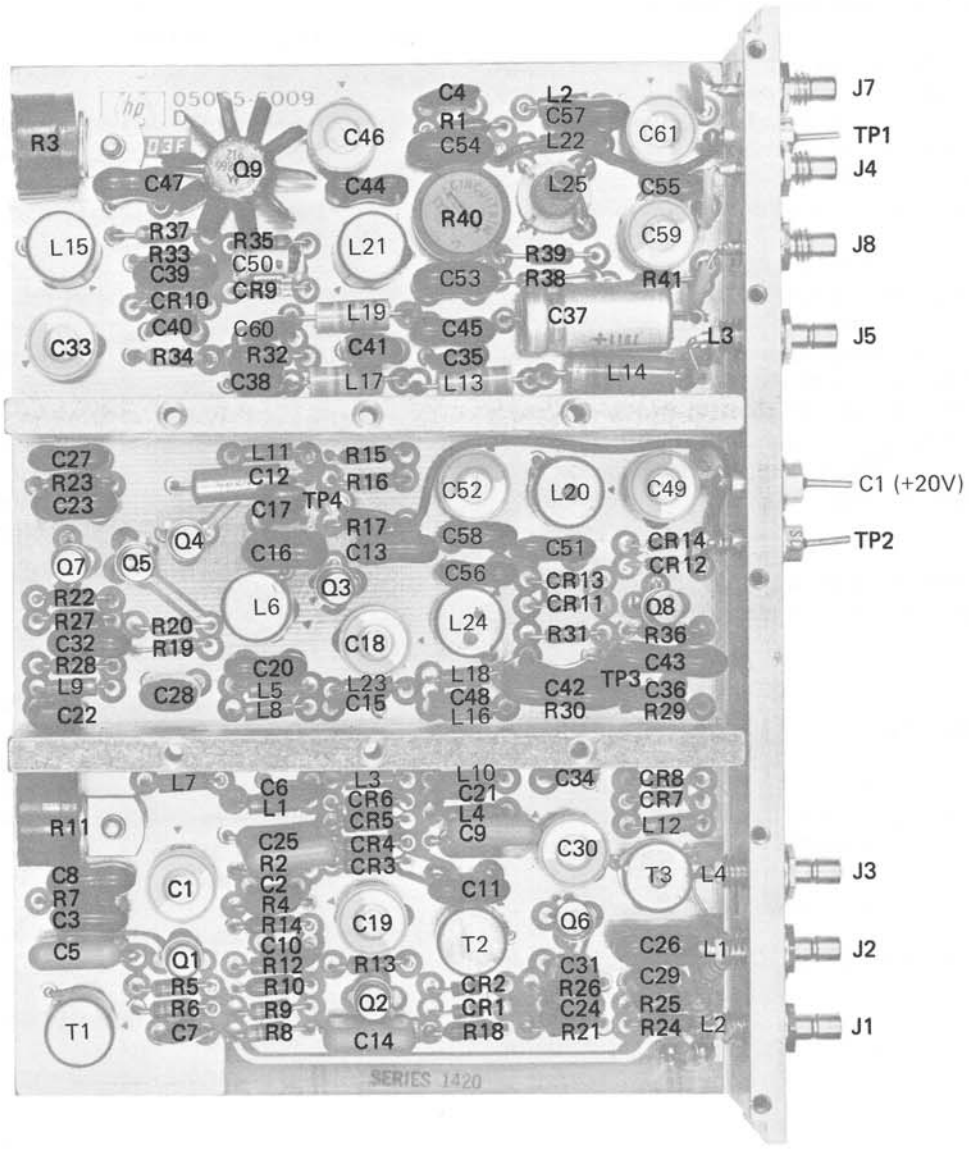
The matching network adjustment must be aligned with the A3 Multiplier installed in the system. See Section 5-25, RF ALIGNMENT under LOOP ALIGNMENT PROCEDURE for adjustment instructions.

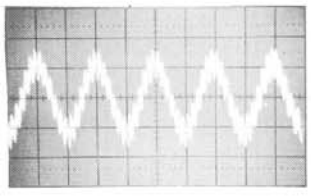
MODULE REPLACEMENT

When replacing the A3 Assembly after repair or when a new A3 Assembly is installed, the instrument should be completely realigned per Section 5-19, LOOP ALIGNMENT PROCEDURE.

Figure 8-11
A3 MULTIPLIER ASSEMBLY

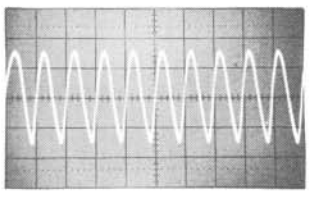
(See Page 8-25)

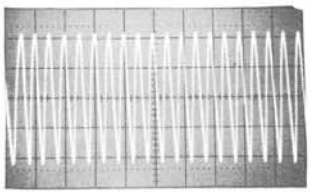




❶ .01 V/cm
.1 μs/cm

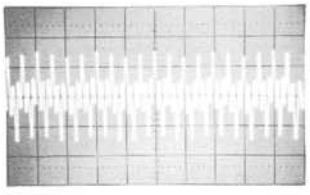
.01 V/cm
.1 μs/cm ❷





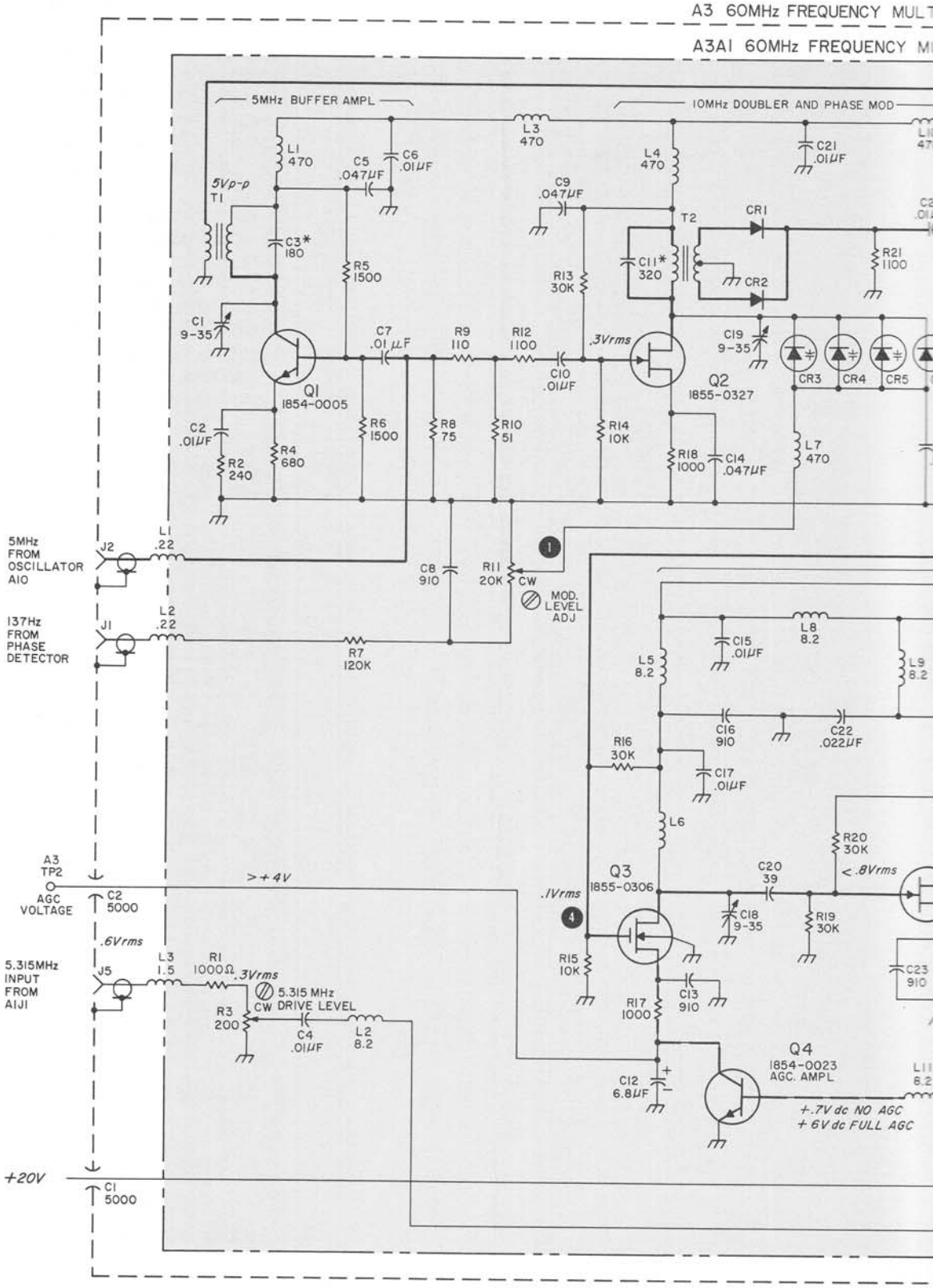
❸ .005 V/cm
.1 μs/cm

.01 V/cm
.1 μs/cm ❹



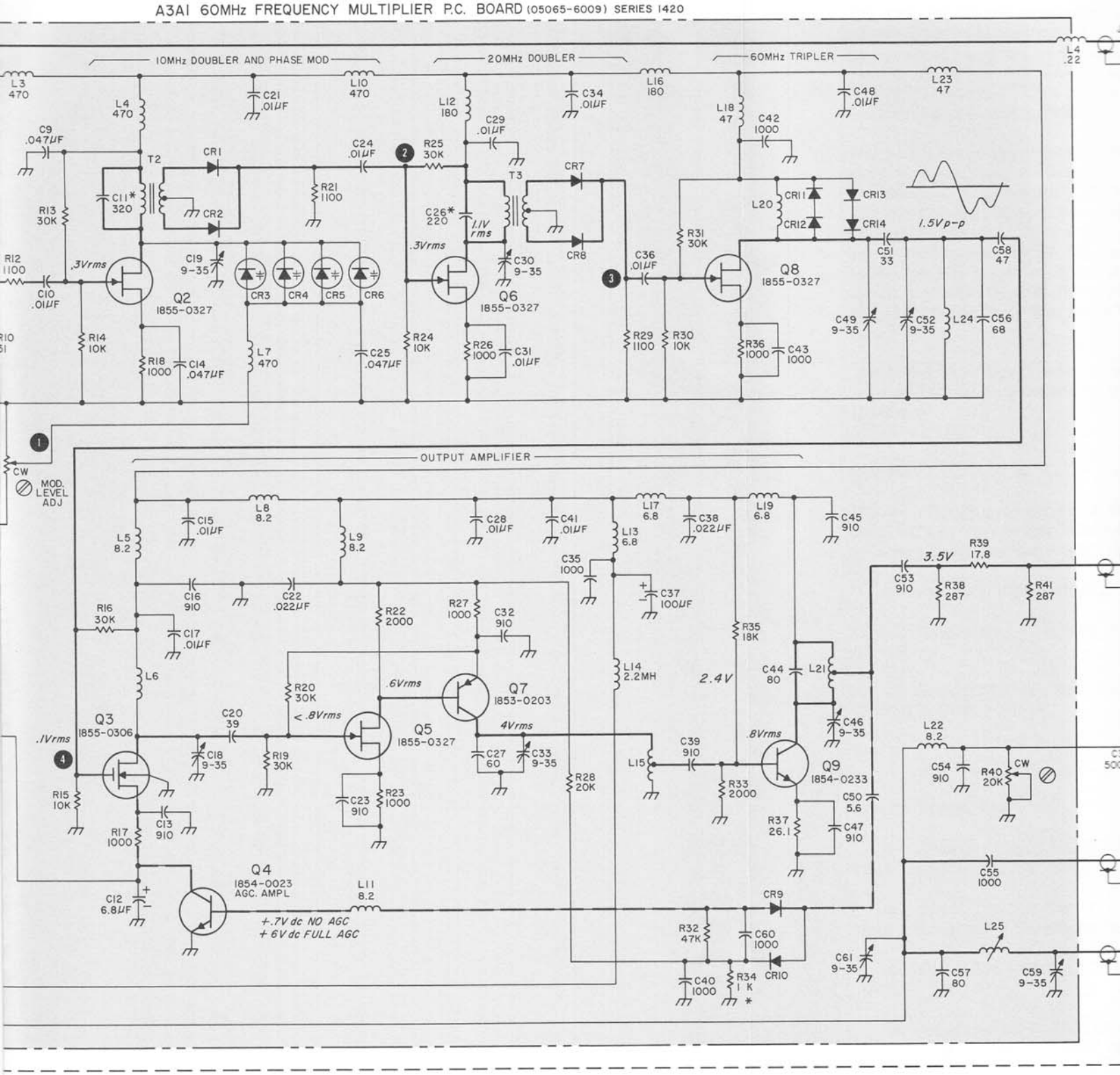
5065A: Normal Operation unless noted.

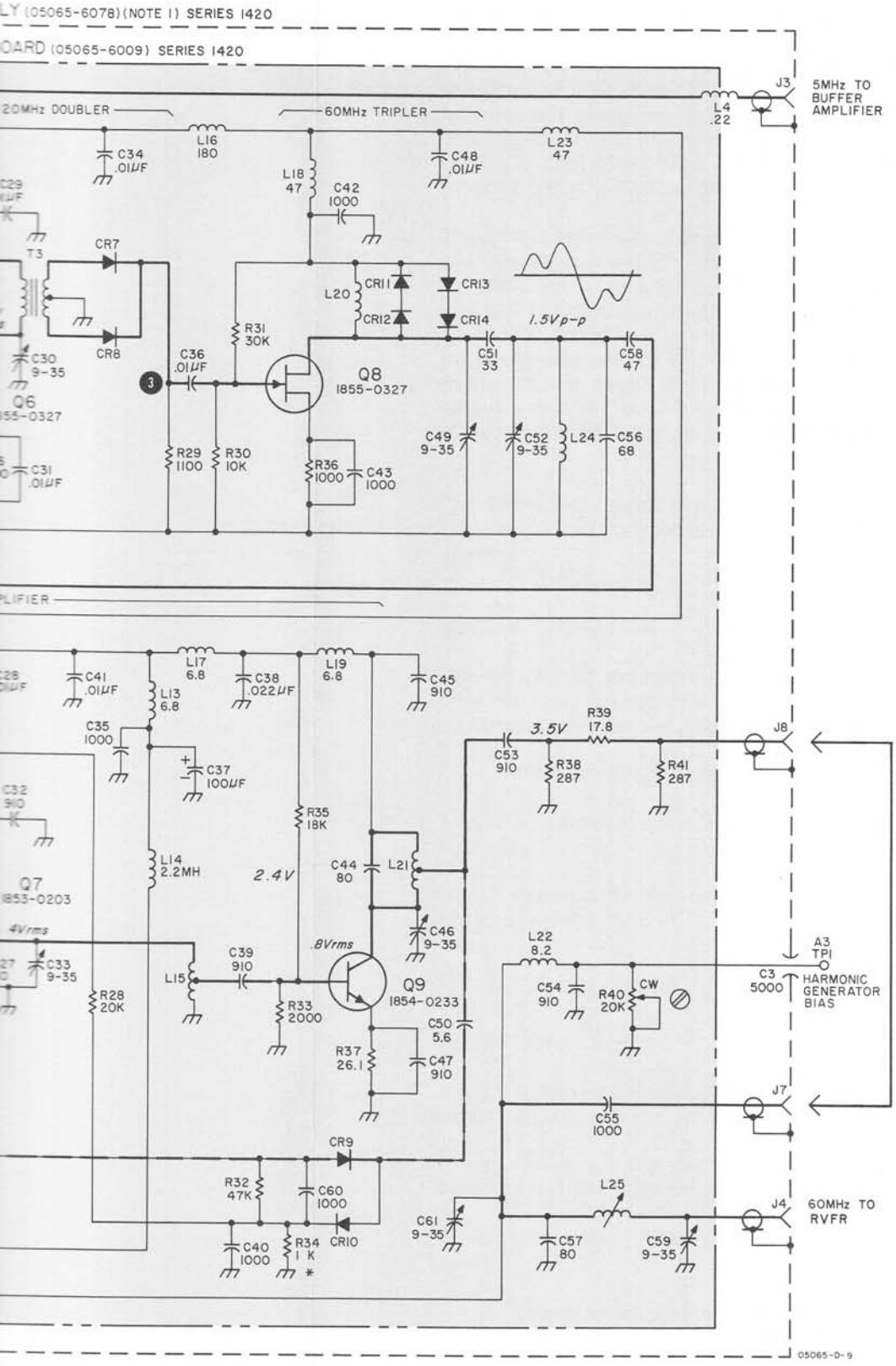
Oscilloscope: DC coupled


A3 60MHz FREQUENCY MULT
A3A1 60MHz FREQUENCY MU
5MHz BUFFER AMPL
10MHz DOUBLER AND PHASE MOD
L1 470
C5 .047μF
C6 .01μF
5Vp-p T1
C3* 180
R5 1500
L3 470
L4 470
C21 .01μF
C9 .047μF
T2
CR1
CR2
C11* 320
R21 1100
R13 30K
C1 9-35
C7 .01μF
R9 110
R12 1100
.3Vrms
C10 .01μF
Q1 1854-0005
Q2 1855-0327
C19 9-35
CR3
CR4
CR5
C2 .01μF
R2 240
R4 680
R6 1500
R8 75
R10 51
R14 10K
R18 1000
C14 .047μF
L7 470
5MHz FROM OSCILLATOR A10
J2
L1 .22
C8 910
R11 20K CW
MOD. LEVEL ADJ
137Hz FROM PHASE DETECTOR
J1
L2 .22
R7 120K
L8 8.2
L5 8.2
C15 .01μF
L9 8.2
C16 910
C22 .022μF
R16 30K
C17 .01μF
L6
R20 30K
A3 TP2
AGC VOLTAGE
>+4V
C2 5000
.6Vrms
Q3 1855-0306
.1Vrms
C20 39
<.8Vrms
C18 9-35
R19 30K
R15 10K
C13 910
R17 1000
5.315MHz INPUT FROM A1J1
J5
L3 1.5
R1 1000Ω
.3Vrms
5.315 MHz CW DRIVE LEVEL
R3 200
C4 .01μF
L2 8.2
C12 6.8μF
Q4 1854-0023 AGC. AMPL
+.7V dc NO AGC
+6V dc FULL AGC
+20V
C1 5000

A3 60MHz FREQUENCY MULTIPLIER ASSEMBLY (05065-6078) (NOTE 1) SERIES 1420

A3A1 60MHz FREQUENCY MULTIPLIER P.C. BOARD (05065-6009) SERIES 1420





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS; INDUCTANCE IN MICROHENRIES
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN.

REFERENCE DESIGNATIONS

A3	A3A1
C1-3	C1-61
	CR1-14
J1-5,7,8	
L1-4	L1-25
	Q1-9
	R1-41
	T1-3
TP1,2	

Figure 8-11. A3 Multiplier Assembly

100 kHz FREQUENCY DIVIDER A4 THEORY

The 100 kHz divider consists of a tuned 1 MHz input amplifier, an integrated circuit decade divider and two tuned output amplifiers. Low pass filters and traps are used to shape the I.C. divider output and to reduce harmonic distortion. The filtered signal drives two tuned amplifiers which provide the sine-wave outputs.

The 1 MHz input signal from A6(9) is amplified by Q1 and saturating transistor amplifier Q4. Decade divider IC1 provides a symmetric 100 kHz square wave at IC1(12). The divided output is amplified and shaped by Q5 and Q7 and is available at A4(14). The divided output is also amplified by Q6, Q8, and Q9 and is available as the 100 kHz output to J1 and J10. A portion of this output is rectified by CR2, filtered by C23, R35, and displayed on front-panel meter at the 100 kHz position.

The 1 MHz input signal is also coupled through emitter-follower Q2 and provides the 1 MHz signal to A5 Digital Divider.

NORMAL OPERATION

The A4 Circuits process the 1 MHz from A6 to produce 100 kHz. An output from A4 is available anytime a 1 MHz signal is fed into A4(6). The A4 outputs are:

a. 100 kHz 1 V/50-ohms at J1 and J10.

b. A buffered 1 MHz output to A5 Digital Divider Assembly.

c. Rectified 100 kHz to CIRCUIT CHECK meter in 100 kHz position.

OPERATIONAL CHECK

a. Observe the CIRCUIT CHECK 100 kHz indication and compare it to Table 5-3.

b. Check for 100 kHz, 1 V rms into 50-ohms at front and rear panel 100 kHz jacks.

c. Check for 1 MHz, .5 V rms into 1 K-ohms at A4(2).

d. Check for no outputs above steps a, b, c, and d when 5 MHz is disconnected or when 1 MHz input signal is removed.

e. Check for 100 kHz and 1 MHz at A4 outputs when 1 MHz input signal is reapplied.

f. Check that the 100 kHz output at J1 and J10 meet specifications as follows:

1) Using the 5065A 5 MHz output as an external time base input to a counter connect the 100 kHz front-panel jack to the counter input and check for 100 kHz ± 1 count. Disconnect the counter.

2) Connect the front panel 100 kHz jack through a 50-ohm feedthrough to an RF voltmeter. Check for 1.0 to 1.5 volts rms. Replace voltmeter with an oscilloscope. Check the 100 kHz output for an undistorted sine-wave. Disconnect the oscilloscope.

3) To check the 100 kHz output harmonic distortion, refer to Table 5-2, steps 4 and 5.

TROUBLESHOOTING

NOTE

For troubleshooting or tuning it will be necessary to mount the A4 circuit card on a HP 05065-6064 circuit board extender. Power should be disconnected before this assembly is removed and reinstalled.

a. Signal Checks

1) To check Q1 and Q4, monitor 1 MHz at IC1(1).

2) To check A2, check for 1 MHz at A4(2).

3) To check IC1, check for 100 kHz at IC1(12).

4) To Check Q6, Q8, Q9, check for 100 kHz, 1 V rms into 50-ohms at A4(11).

b. Tuning Adjustments

1) Connect oscilloscope probe at Q1 collector. Adjust T1 for maximum amplitide at 1 MHz.

2) Connect oscilloscope probe at Q9 collector. Adjust T2 for maximum amplitide at 100 kHz.

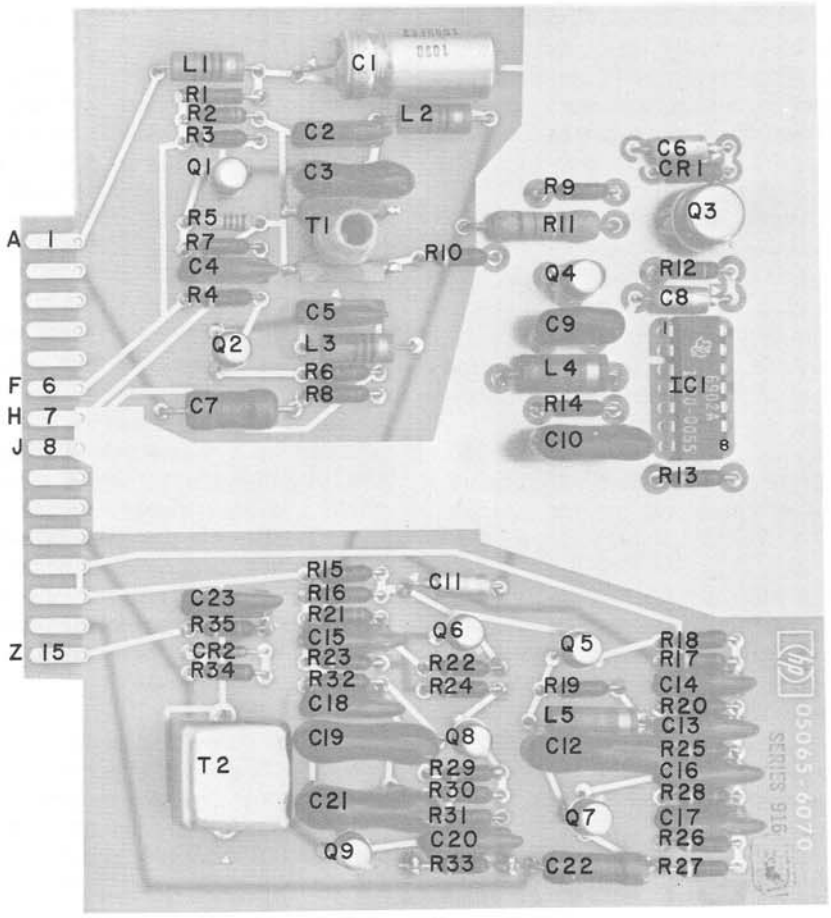
3) Make minor readjustments of T1, T2 for a stable 100 kHz, 1 V rms into 50-ohms at A4(11).

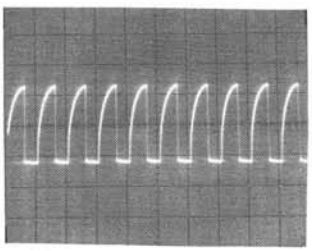
MODULE REPLACEMENT

When replacing the A4 Assembly after repair or when a new A4 Assembly is installed, the circuit should be completely realigned per the preceding paragraphs.

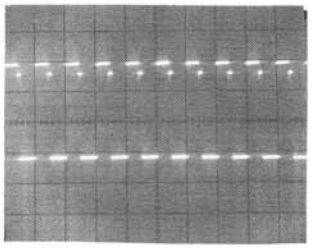
Figure 8-12
A4 100 kHz FREQUENCY DIVIDER

(See Page 8-27)

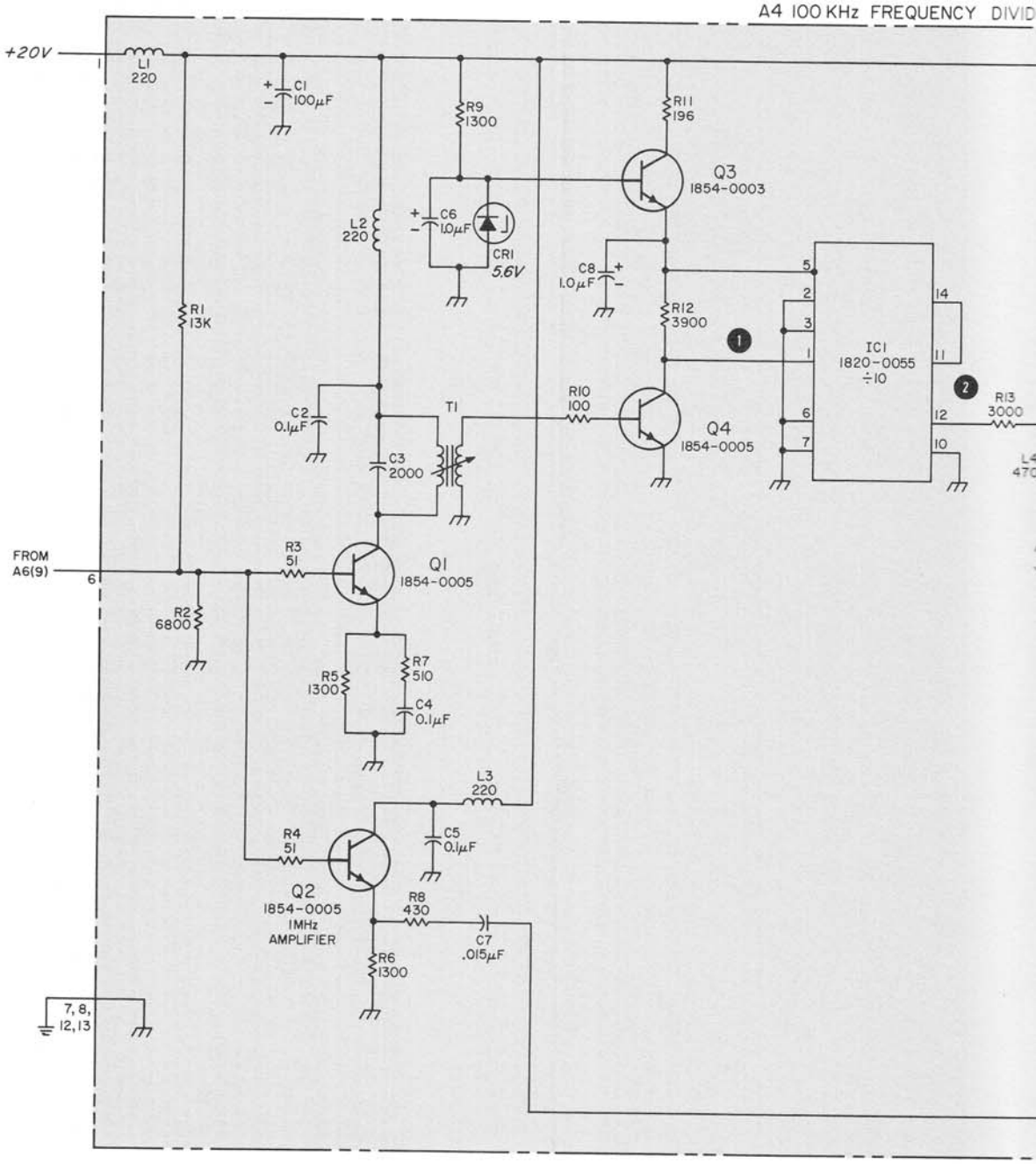




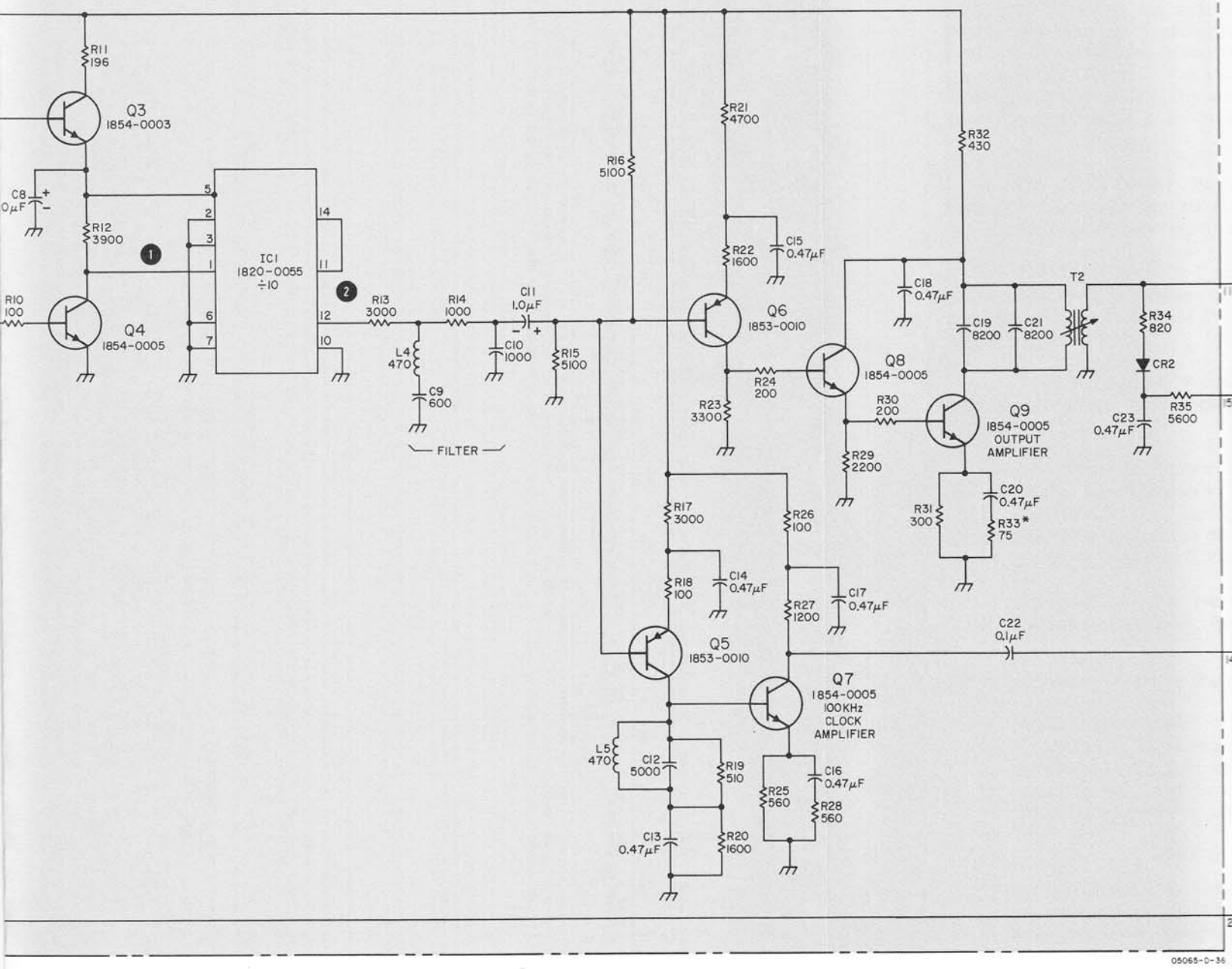
❶ 2 V/cm
1 μsec/cm
dc coupled



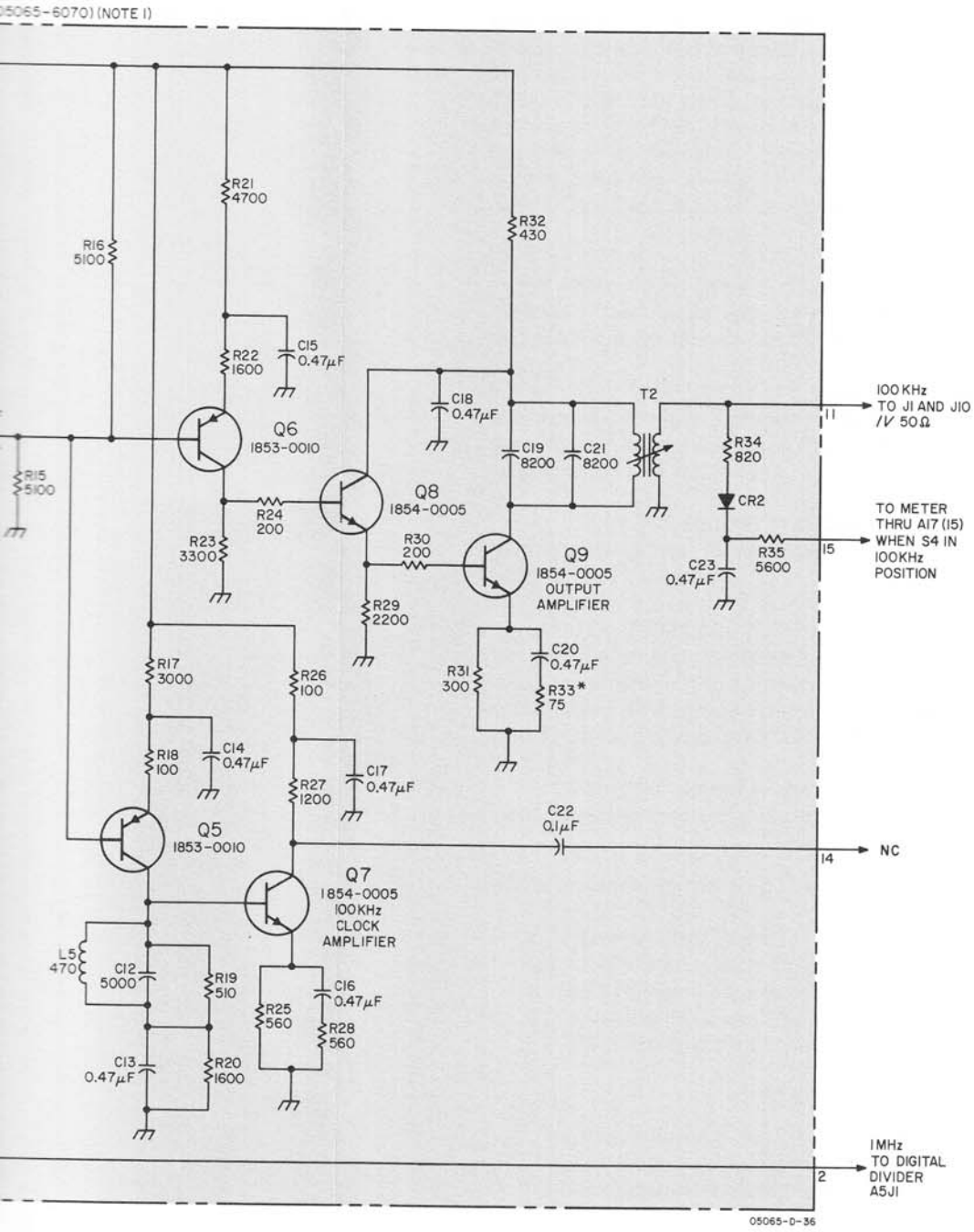
❷ 1 V/cm
10 μsec/cm
dc coupled


A4 100 KHz FREQUENCY DIVID
+20V
1
L1
220
C1
100μF
R9
1300
R11
196
Q3
1854-0003
L2
220
C6
1.0μF
CR1
5.6V
C8
1.0μF
R1
13K
R12
3900
5
2
3
1
IC1
1820-0055
÷10
14
11
12
10
6
7
R13
3000
R10
100
Q4
1854-0005
C2
0.1μF
T1
C3
2000
FROM
A6(9)
6
R3
51
Q1
1854-0005
R2
6800
R5
1300
R7
510
C4
0.1μF
L3
220
R4
51
C5
0.1μF
Q2
1854-0005
1MHz
AMPLIFIER
R8
430
C7
.015μF
R6
1300
7, 8,
12, 13

A4 100 KHz FREQUENCY DIVIDER ASSEMBLY (05065-6070) (NOTE 1)



05065-D-36



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS; INDUCTANCE IN MICROHENRIES
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN

REFERENCE DESIGNATIONS

A4
C1-23 CR1, 2 IC1 L1-5 Q1-9 R1-35 T1, 2

Figure 8-12. A4 100 kHz Frequency Divider

DIGITAL DIVIDER A5 THEORY

GENERAL DESCRIPTION

In instruments equipped with Time Standard Option 001 or 003, digital divider circuits provide 1 PPS for A16 Assembly (also part of Time Standard Option) which in turn provides two outputs: (1) 1PPS "tick" pulses at the front-panel 1 PPs jack and, (2) the push-pull clock drive for the front panel mechanical clock. Input to A5 module is the internally connected 1 MHz signal from the Frequency Dividers. The top cover is removed for access to A5 controls and the mechanical clock adjustment. Time Standard Option 001 controls are as follows:

a. The TIME DELAY thumbwheel switch on A5 module. This control has six thumbwheels for 1 μsec to 1 sec incremental delay of the output "tick" pulse.

b. The TIME DELAY 0-1 μsec screwdriver adjustment on A5 module provides continuous delay control over any 1 μsec portion of the TIME DELAY thumbwheel switch setting.

c. The FAST and STOP pushbuttons on A5 module permit setting the mechanical clock to the nearest second.

d. The SYNC pushbutton on A5 module is used for automatic synchronization of the output 1 PPS "tick" pulse within 9 to 11 μsec of an external reference sync pulse. This sync pulse must be greater than +5 V with a rise time of less than 0.05 μsec.

e. The "set" knob at the rear of the mechanical clock provides for minute and hour adjustment.

Five subassemblies make up the overall assembly:

a. A5A1 Adapter Board
b. A5A2 Master Clock Board
c. A5A3 Preset Clock Board
d. A5A4 Switch Circuit Board
e. A5A5 Interconnect Board

NOTE

In the following paragraphs, add"A5" to the reference designations used for a complete reference designation. Example: A3IC3 = A5A3IC3.

The 1 PPS "tick" clock pulse and 1 PPS clock-drive output are generated by: (1) digital division and, (2) both incremental and continuous delay. This technique, illustrated by the A5 Block Diagram provides for 0 to 1 sec delay of the 1 PPS "tick" output.

1 MHz from a buffer amplifier in the A4 module connects to the master clock. This master clock section is a 10^{-6} decade counter which produces 1 PPS pulses. The 1 PPS pulses activate the preset clock which delivers a digitally delayed 1 PPS pulse. The preset clock provides for delay in increments of 1 μsec up to 1-second. The TIME DELAY thumbwheel switches provide the preset delay information. Continuously variable delay over a zero to 1 μsec period is furnished by the zero to 1 μsec TIME DELAY control working in conjunction with an adjustable one-shot multivibrator. The variable delay adds to the incremental delay to provide fully adjustable delay from zero to one full second.

With the reset gate open, 1 MHz pulses are processed in the input filter shaper and applied through the reset gate to 1 MHz MV A2IC2 as shown in the Functional Block Diagram. This IC drives master preset clock MV A2IC3 and also delivers a 0.2 μsec pulse to output gates A3IC2 and A3IC12B. A2IC3 feeds 0.2 μsec, 1 MHz pulses to the master clock and the preset clock as count pulse inputs.

The master clock consists of six, serially-connected, divide-by-10 decades for a 10^{6} division, thus producing the 1 PPS output. These 100 msec, 1 PPS output pulses initiate reset and preset of the preset clock. When actuated by a master clock pulse, reset one-shot mV A3IC15 delivers a 1.3 μsec reset pulse to the preset clock, and also triggers preset one-shot mV A3IC16. This IC delivers a 0.5 μsec preset pulse to the thumbwheel switch circuits to preset thumbwheel binary information into the preset clock and thus produce the required delay. A coincidence output from NOR gate A3IC17B holds the preset clock input closed during the reset and preset period.

At the end of the reset and preset period, 1 MHz pulses from A2IC3 drive the preset clock until the total of preset counts plus the number of 1 MHz pulses = a 999,999 count. At this time, the 9's detector circuit provides the necessary inputs to AND gate A3IC12A for a 1 μsec, 1 PPS output. This is the gating signal for A3IC2C.

This 1 PPS output is incrementally delayed by the thumbwheel switch setting. The second input to AND gate A3IC2C is the train of 1 MHz pulses from A2IC2. Coincidence between A3IC2C inputs produces a 0.2μsec output that connects through NOR gate A3IC2D to the variable delay circuit on A5A4 circuit board and to the clock drive amplifiers.

Variable delay from 0 to 1 μsec is furnished by the TIME DELAY screwdriver control to adjust variable one-shot mV A4IC1. The amplified A4Q1 output connects through J3 to A16 module where the 1 ((S pulse is shaped and narrowed for the "tick" output at the front panel 1 PPS jack.

The other output of A3IC2D is amplified by Q13 and Q15 for an output to the clock drive circuit in A16 module. To speed up the clock drive output, the FAST pushbutton is depressed for a 10-PPS output. To slow down the clock, the STOP pushbutton shorts the clock output to ground when depressed.

CIRCUIT DESCRIPTION

The 1 MHz drive signal connects through J1 to A5A2(1) Master Clock Board. The master clock board has the following circuits:

a. Input Filter and Shaper Circuit
b. Sync One-Shot mV Circuit
c. Gated 1 MHz mV and the Master and Clock Drive mV
d. Master Clock (six decades connected for a 10^6 division)

INPUT FILTER AND SHAPER

Diodes A2CR1 and A2CR2 limit input signal level. A2Q1 and A2Q2 drive the 1 MHz high "Q" filter to suppress unwanted signals. A2C4 resonates T1 at 1 MHz. CR3 provides regulated bias for A2Q1. In the filter circuit, A2C9 tunes A2Y1 to 1 MHz. The spectrally clean 1 MHz signal from A2Y1 is applied to shaper amplifiers A2Q4 and A2Q6 to drive gated 1 MHz MV A2IC2. Diode A2CR5 and saturating amplifier A2Q6 provide the shaping (squaring) action.

GATED 1 MHz MULTIVIBRATOR

A2IC2 produces a 1 MHz, 200 nsec wide, positive pulse for 1 MHz clock drive MV A2IC3. This pulse also goes to the output gates on A5A3 circuit board [A5A2(4) to A5A3(5)] to A5A3IC2C(1) and to A5A3IC12B(9). When proper gate sequencing occurs, this pulse is gated through A3IC2C or through A3IC12B (as shown in the timing diagrams) to the 1 PPS output circuits.

The 1 MHz master and preset clock multivibrator A2IC3 is triggered by the negative transition of A2IC2 output pulse, producing a negative 1 MHz output pulse at A2IC3(7) delayed by 150 nsec. This pulse is the count pulse for the master and preset clock.

The master clock is a six-decade divider producing a negative, 100 msec wide, 1 PPS output. This master pulse controls the reset and preset circuits of the preset clock divider. Since all decades of the master clock are identical, only A2IC6 will be discussed.

Normally, decade dividers are allowed to fill until the count cycles to "0". At this time, an output pulse is applied to the next decade. Thus, for each 10 inputs, 1 output pulse is applied to the next stage. However, this technique introduces error due to decade cycling time and decade temperature sensitivity. This error is accumulative through a divider chain and, with 6 decades, could amount to as much as 1 μsec. The technique used in the master clock divider reduces this error to less than 100 nanoseconds.

An "H" input pulse at A2IC6(5) is necessary for the decade to divide; therefore, all count inputs to the inverter A2IC4A(1) must be "L". When the decade is at "0", voltage levels at pins 6, 7, 8, and 1 are "H" and output NAND gate A2IC12A(6) will be "L", applying a "L" count pulse to the following decade inverter. If any input signal to NAND gate A2IC12A is "L", the following decade inverter will receive an "H" which will not count.

The 1 MHz "L" pulses applied to A2IC4A(1) are inverted and applied to divider, A2IC6. As the count progresses within the IC, pins 6, 7, 8, and 1 will change from "H" to "L" at various counts as shown in the timing diagram for A2IC6. When the tenth count pulse is applied to A2IC6(5), the divider cycles to "0" and A2IC6 (6, 7, 8, and 1) place an "H" at A2IC12A (1, 2, 4, and 5). However, A2IC12A(6) is still "H" because the same pulse cycling the decade to "0" places an "L" through A2CR6 to the NAND gate, holding it closed. When this pulse goes "H", the NAND gate applies an "L" to the following decade input inverter as a count pulse. This state will remain until the next "L" count pulse, "1", is applied to A2IC4A(1). A2IC12A(3) goes "L", closes the gate and ends the "L" input to the following decade input inverter. Since the actual output pulse was not processed through the decade, delay due the decade is eliminated.

This process is repeated through the five remaining decades with the final output master tick, 1 PPS, 100 msec, negative pulse applied to the following preset clock divider and associated circuits.

RESET AND PRESET ONE-SHOT CIRCUITS

Operation of Digital Divider A5 is illustrated in the A5 timing diagrams. The 1 PPS master clock tick triggers reset one-shot A3IC15 producing complementary 1.3 μ sec pulses at pins 7 and 10. The "L" signal at pin 7 drives reset amplifiers A3Q7, A3Q9, A3Q11, and decade control NOR gate A3IC17B through inverting amplifier A3IC17A. This signal resets decade A3IC3, A3IC4, A3IC5, A3IC6, A3IC7, and A3IC8 to "0". During the decade reset time, A3IC17B(7) output holds all decade input NAND gates closed to any input count. Each time the reset one-shot is triggered, a 1.3 μsec "H" signal is also placed at NAND gate A3IC12B(10).

When the complementary 1.3 μsec pulse at A3IC15(10) goes "L", it triggers preset one-shot A3IC16. The output at pin 10 of A3IC16 is inverted by A3Q8, A3Q10, and A3Q12 applying a 0.5 μsec "L" preset pulse into the thumbwheel switches to preset the desired count into the preset clock. The same signal at A3IC16(10) causes NOR gate A3IC17B(7) to remain "L" an additional 0.5 μsec, which holds the decade input NAND gates closed to any input count during this presetting action. The preset clock decades are now reset and preset.

PRESET CLOCK DIVIDERS

Six adjustable decade dividers make up the preset clock divider. The dividing scheme allows division by any integer between 1 and 10^6 by simply setting TIME

DELAY thumbwheel switch S1A through S1F. This adjusts the divider output phase from 1 μsec to 1 sec. The phase adjustable output pulse is a 1 PPS, 1 μsec, "L" signal at 9's detector NAND gate A3IC12A(6), applied to inverter A3Q6 and gate around one-shot A3IC13(9). The relationship between the 1 MHz input, the master clock 1 PPS output, and the preset clock 1 PPS, 1 μsec, output "L" pulse can be seen in A5 Digital Divider Timing Diagrams.

The standard decade divider provides one output pulse for each 10 input pulses. Preset divider A3IC3 provides an output pulse through NAND gate A3IC9 to 9's detector A3IC12A(5) and to the following decade when the preset count plus the input count total "9" (input to following stage occurs at "8" and continues through "9"). Operation of A3IC3 is the same as that shown in the timing diagram for A2IC6 decade.

When the decade count is "0", all binary outputs are "H" but as the count progresses, levels at pins 6, 7, 8, and 1 change state depending on the number of pulses into the decade. At the count of "9", pins 1 and 6 are "L" (representing "9") and pins 7 and 8 are "H". The next input pulse "10" will cycle the decade to "0" and the count begins again.

To change the decade to a divide-by-2 divider; when the decade state is "0" (pins 6, 7, 8, 1 "H") and before any input signal is applied to pin 5, pulses are applied to pins 6, 7, and 8 driving them "L". The decade state is now "7" before any input signal is applied. The first 2 input pulses cause pins 6 and 1 to go "L" and a "9" is sensed at the output IC9A(3, 5). Thus, with only two inputs there is an output or divide-by-2 action.

The preset clock divider chain may be set to divide by any integer from 1 to 10^6 by setting the complement 9 into the decades prior to the counting sequence. This is done automatically by TIME DELAY thumbwheel switch S1A through F. Whatever time delay is set on the switch, the complement "9" is set into the preset clock dividers prior to counting.

Assume a 1 μsec delay is set on the thumbwheel switch; this presets 999998 into the dividers (switch setting is 000001). When the master clock has completed its counting sequence, the master tick output triggers the reset and preset circuits in the preset divider section. During reset and preset time, preset divider decade inputs are held closed. During preset time, 999998 is set into the decades via the thumbwheel switch and "H" signals are preset at A3IC12A(2, 3, 1, 4). However, this gate will not change state since an "L" is present from A3IC9A(6) (this decade has the count of "8").

The first decade receives the first count pulse causing A3IC9A(6) to go "H" which causes A3IC12A(6) to go "L" until the next input pulse to A3IC1A(13) which arrives 1 μsec later. The 1 sec "L" signal is inverted by A3Q6 and applied as an "H" pulse to NAND gate A3IC2(2). The next gated 1 MHz output pulse from A2IC2 will also place an "H" signal at A3IC2C(1). This causes gate A3IC2C to change state and apply an "H" signal through NOR gate A3IC2D to the 0-1 μsec variable delay mV on A5A4 Switch Board Assembly.

If a delay of 2 μsec is desired, the sequence of events is the same except 999997 would be the preset input information. Instead of the first pulse into A3IC3(5) causing A3IC12A to change state, the second pulse causes the state change; thus, the pulse applied to the 0-1 μsec delay MV on A5A4 circuit board is changed in phase by an additional microsecond. This same sequence of events occurs for all switch settings except 999999.

When 999999 (note the A5 timing diagram) is set on the thumbwheel switch, no preset information is set into the dividers and they divide by 10^6. When this occurs, the preset clock and master clock are dividing by the same number. The dividers reach a count of 999999 and a small pulse is produced at A3IC12A(6). This pulse triggers gate around one-shot A3IC13, producing an "H" 1.1 μsec pulse that is applied to A3IC12B(12). When the master tick goes "L", A3IC12A(6) goes "H" and A3IC15 reset one-shot is triggered. This places another "H" pulse at NAND gate A3IC12B(10). With two of the required three inputs present, the next gated 1 MHz pulse will gate through A3IC12B(9) and NOR gate IC2D to the output circuits.

The 1 PPS output at A3IC2D(6) connects to A5A4 Switch Circuit Board and is processed by variable delay one-shot MV A4IC1 for a 0-1 μsec time delay. This screwdriver adjustment provides continuous control over the 0-1 μsec period. The delayed output pulse connects from amplifier inverter A4Q1 to the "tick" blocking oscillator in the A16 Digital Divider Power Supply module which delivers the 1 PPS "tick" pulse to the front panel jack.

For the clock-drive output, A3IC2D(6) 1 PPS output is amplified by A3Q13, A3Q14, and A3Q15, and routed to the clock drive amplifier on A16 Digital Divider Power Supply. When the STOP pushbutton is depressed, A3Q15 clock drive output is grounded to stop the front panel clock. When the FAST pushbutton is depressed, preset divider A3IC8 input pulses are routed through A5S1 to A3Q14 for a 10 PPS clock drive output. This speeds up the front panel clock to advance it.

The 1 PPS output is synchronized to an external pulse by pressing SYNC pushbutton A5S2. This allows the external pulse feeding in from SYNC jack A5J5 to trigger one-shot MV A2IC1, resetting the master clock through A2Q5 to "0" and holding the input to gated 1 MHz one-shot mV A2IC1 off for 7.3 μsec. At the end of the 7.3 μsec period, the counting sequence will start. Resistor A2R16 and capacitor A2C10 are adjusted for the 7.3 μsec period.

A5 MAINTENANCE

NORMAL OPERATION

Digital divider circuits provide one pulse-per-second output ticks available at front and rear panel 1 PPS BNC output jacks. The divider drive is an internally connected 1 MHz signal from Frequency Divider Assembly A6. Option 001 circuits also provide drive for front panel digital clock.

OPERATIONAL CHECK

Complete operational check is given in Table 5-2, item 7.

TROUBLESHOOTING

The entire digital divider assembly may be removed and reconnected for troubleshooting. Extender board (HP Part No. 05061-6073) furnished, makes circuit board components available for testing.

Digital divider power supply common is isolated from instrument common. To observe waveforms and measure divider voltages, divider common may be connected to instrument common for troubleshooting with no adverse effect. However, this connection must be removed when divider is reassembled.

Each circuit board inputs and outputs are available on interconnection board assembly A5A5. Thus, trouble may be isolated to one specific board assembly before disassembling the entire unit. Troubleshooting table and schematic diagrams provide troubleshooting information.

Periodic adjustments to divider circuits are not necessary. When adjustable components or components related to adjustable components are replaced, the following adjustments should be made.

a. A5A2T1 Adjustment. With instrument in normal operation (frequency divider on) connect RMS Voltmeter to A5A2T1 secondary. Adjust A5A2T1 for maximum voltage indication on voltmeter.

b. A5A2C9 Adjustment. With instrument in normal operation (frequency divider on) connect oscilloscope to A5A2Q6 collector. Adjust A5A2C9 for most symmetrical square wave observed on oscilloscope.

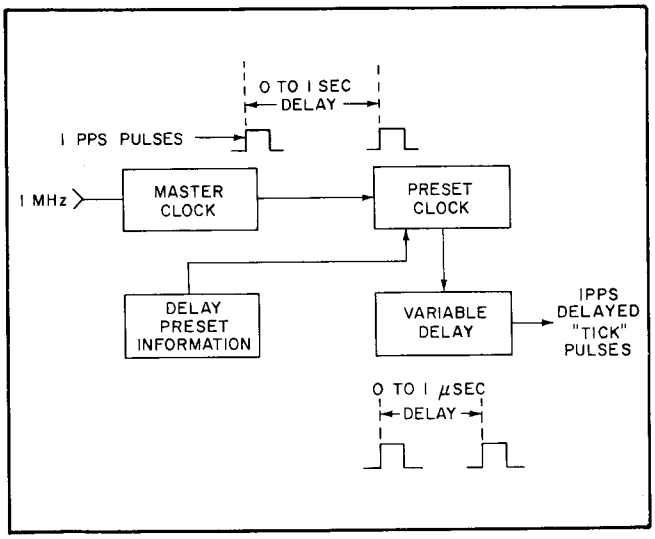
c. A5A2C10 Adjustment. With instrument in normal operation (frequency dividers on) set TIME DELAY thumbwheel switch to "000000" and 0-1 μsec TIME DELAY adjust to max. cw. Externally synchronize digital divider circuits (Paragraph 3-23). Using an oscilloscope, compare external synchronization pulse with 1 PPS output pulse. Adjust A5A2C10 for 10 μsec 1 PPS delay ± 1 μsec.

Troubleshooting Table

Will not synchronize to external pulse.	Check external pulse characteristics (Table 1-3). Check sync cir cuitry A5A2 (Q3, IC1, Q5, and Q7).
Incorrect output pulse shape.	Check output circuits (A16) A5A4 (IC1, Q1), (Q7 and Q10), and 13.3 V supply (A16).
TIME DELAY switch does not affect output pulse time delay.	Check each switch position (Table 5-2, Item 7). If symptom is in only 1 or 2 switch positions, check preset circuitry associated with those positions including preset coupling diodes and the associated decade. If symptoms are present regardless of thumbwheel settings, refer to Table 5-6. If output stops only when thumbwheel setting is "999999" trouble is probably in A5A3 (IC13,IC12B, or IC2D).

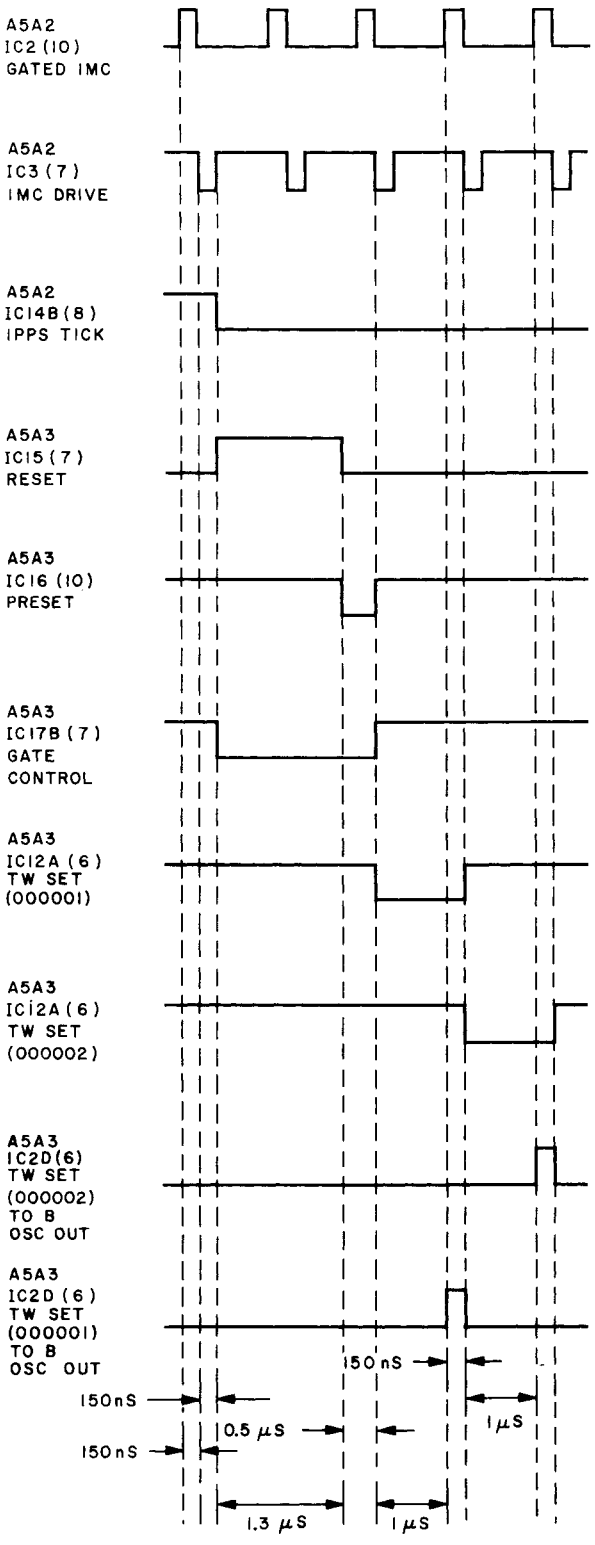
MODULE REPLACEMENT

No adjustments required when Digital Divider Assembly or circuit board assemblies are replaced.



Digital Divider Timing Diagrams

(Thumbwheel switch set at 000001)



(Thumbwheel switch set at 999999)

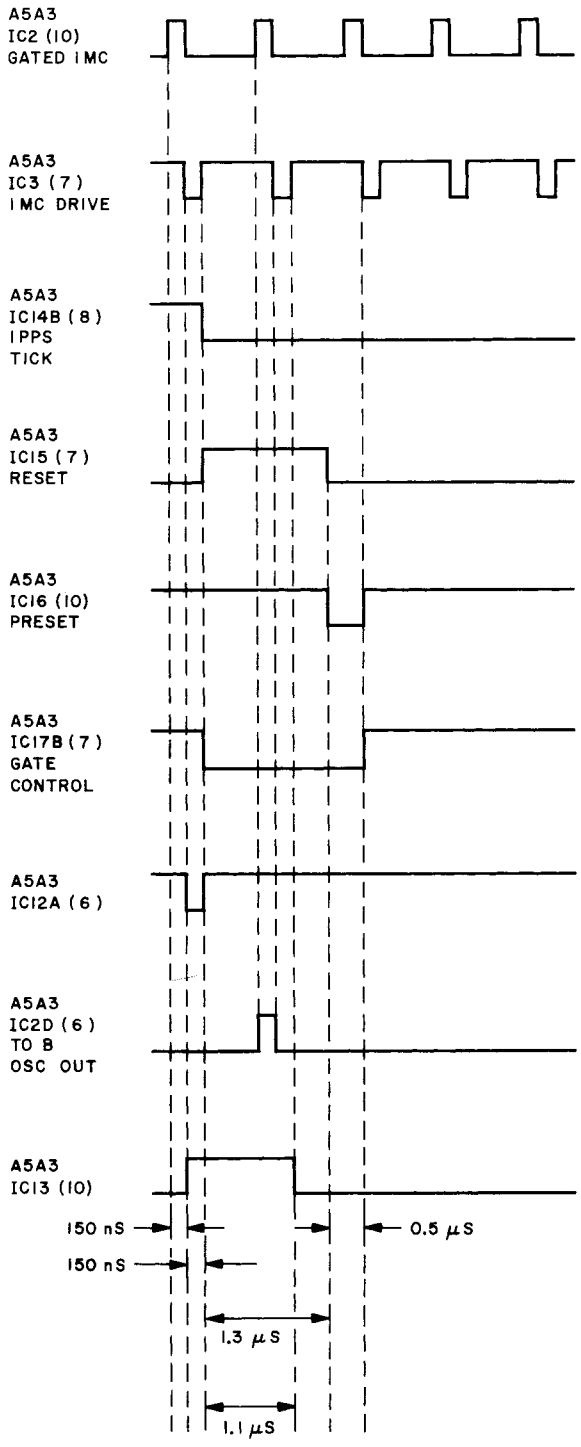
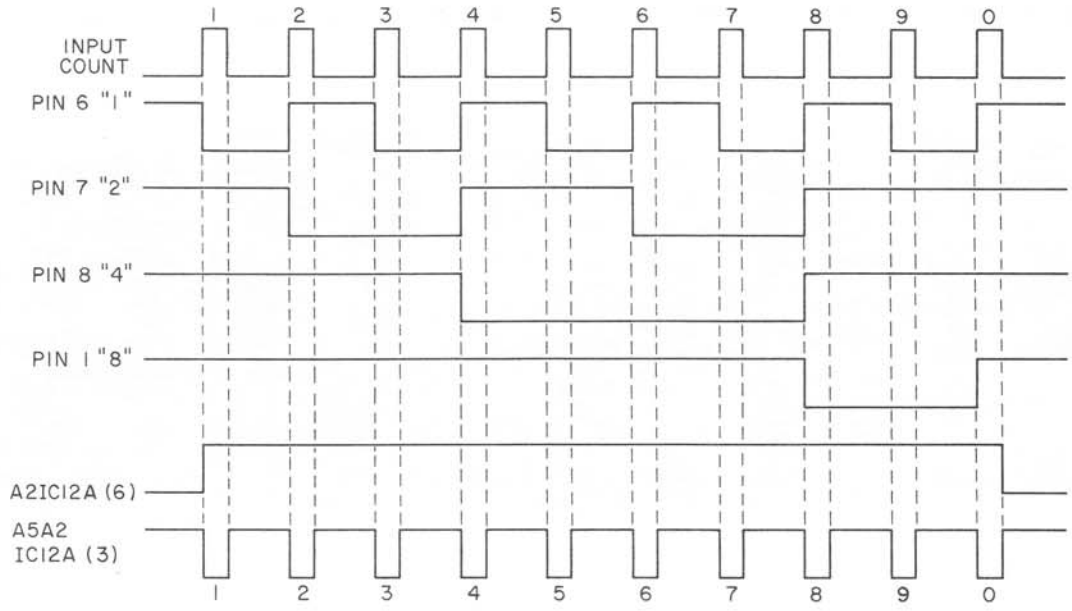
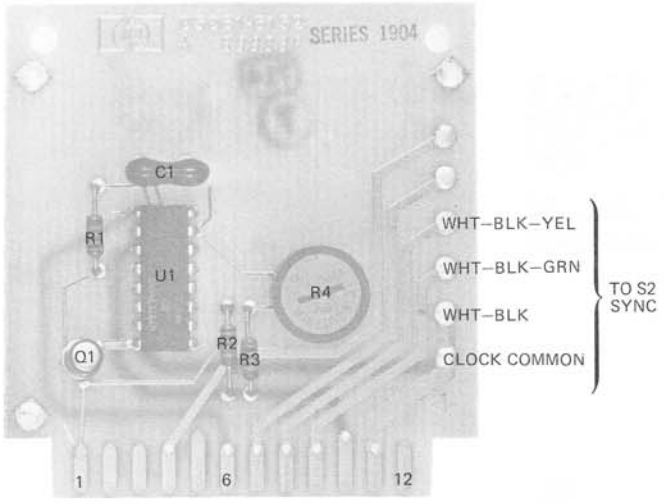
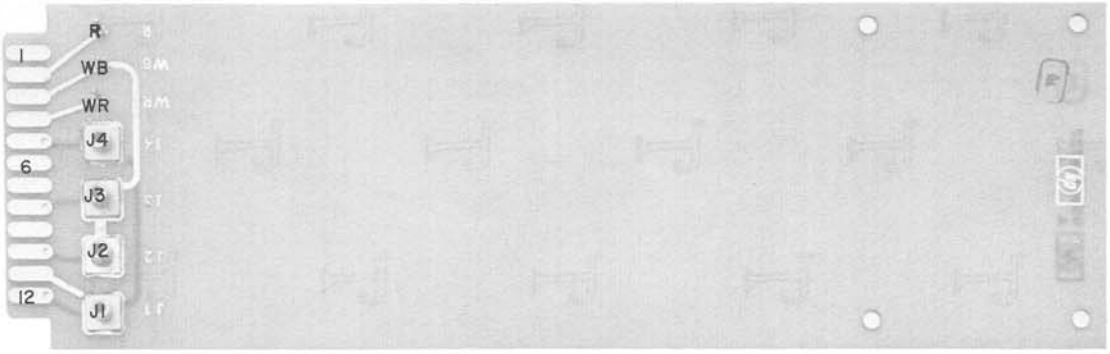


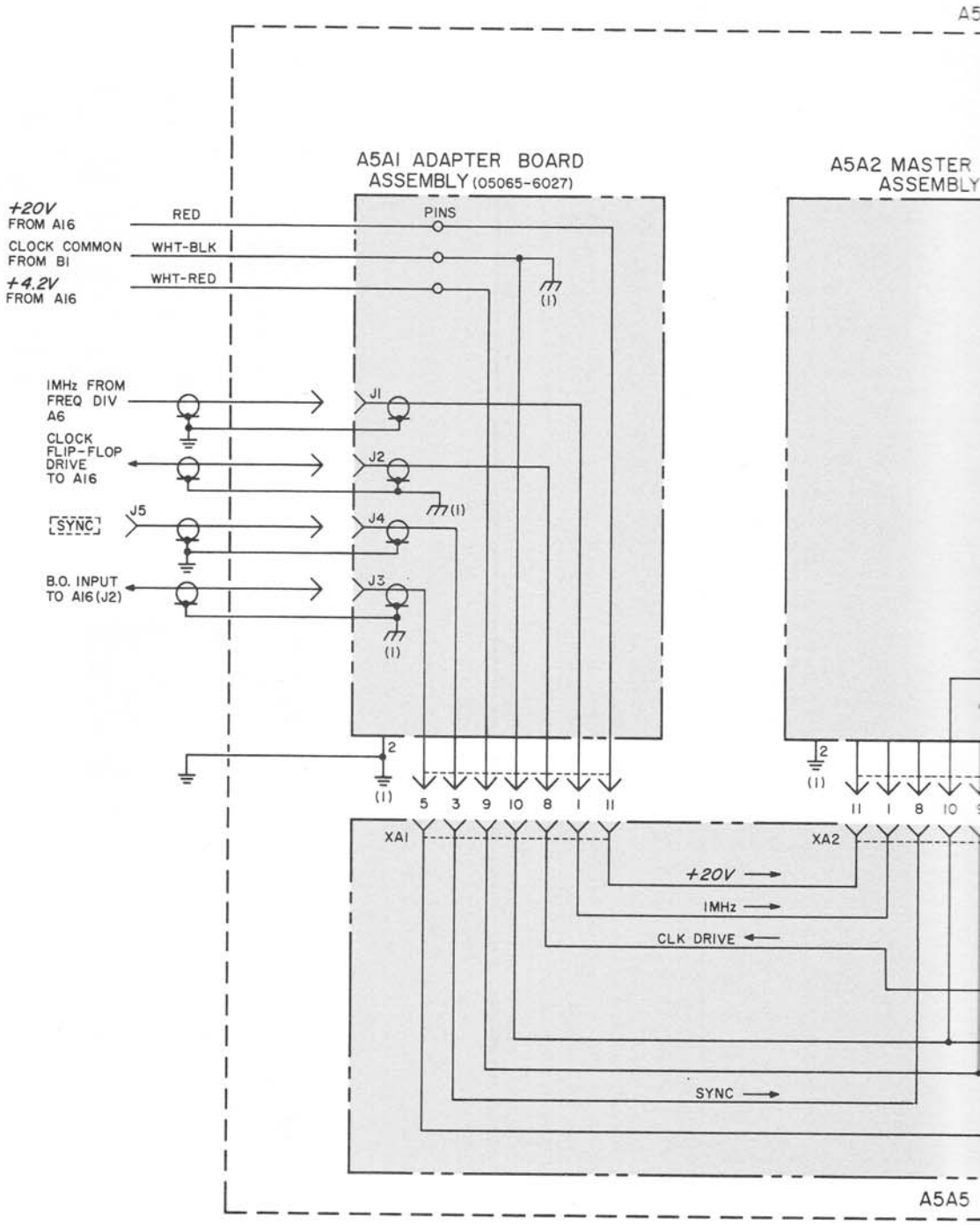
Figure 8-13
A5 DIGITAL DIVIDER ASSEMBLY (OPTION 001)
(Sheet 1 of 3)

(See Page 8-33)


1 2 3 4 5 6 7 8 9 0
INPUT COUNT
PIN 6 "1"
PIN 7 "2"
PIN 8 "4"
PIN 1 "8"
A2IC12A (6)
A5A2 IC12A (3)
1 2 3 4 5 6 7 8 9 0

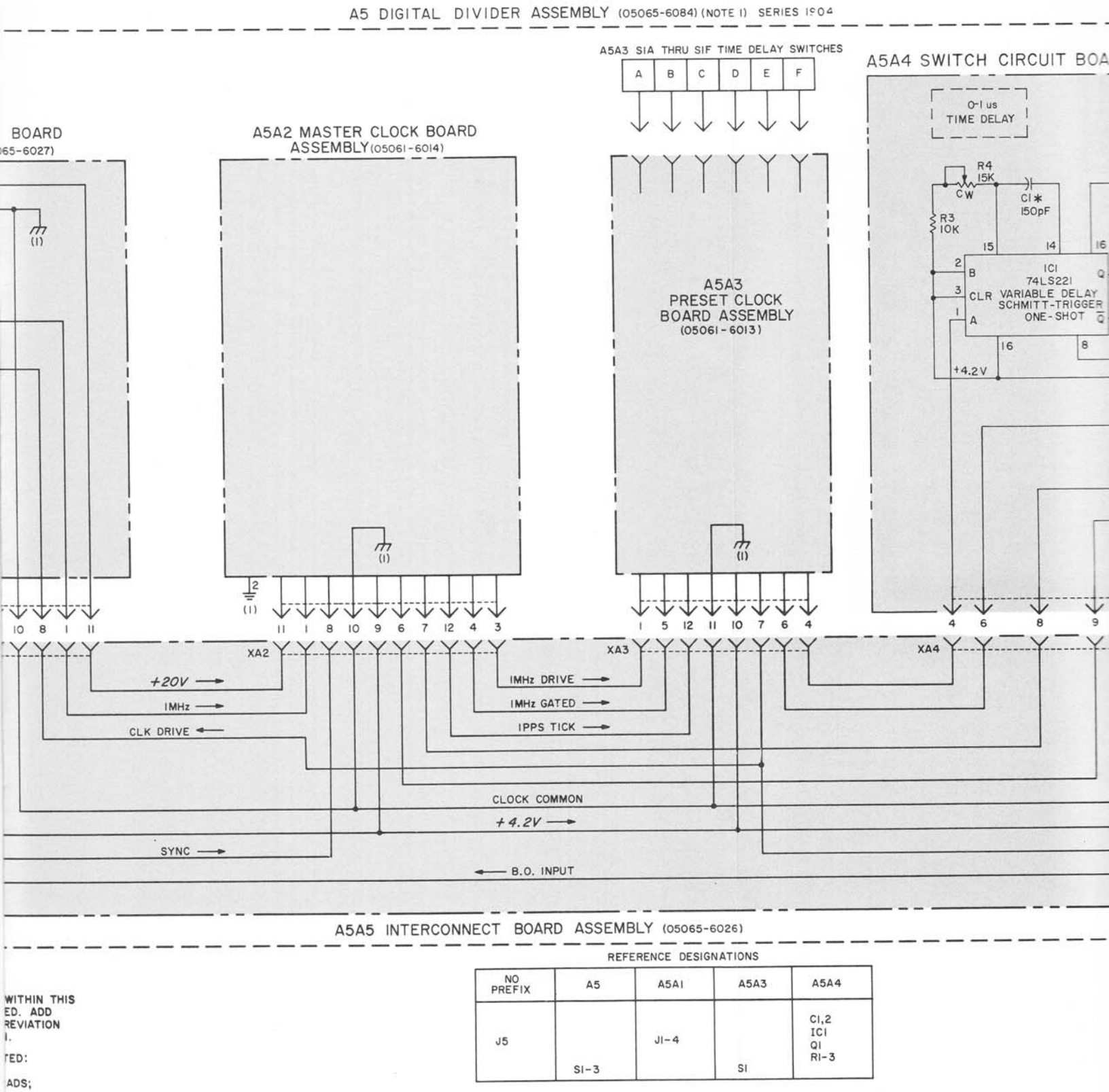

SERIES 1904
C1
R1
U1
R4
Q1
R2
R3
WHT–BLK–YEL
WHT–BLK–GRN
WHT–BLK
CLOCK COMMON
TO S2 SYNC
1
6
12


R
WB
WR
J4
J3
J2
J1
1
6
12



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN.



REFERENCE DESIGNATIONS

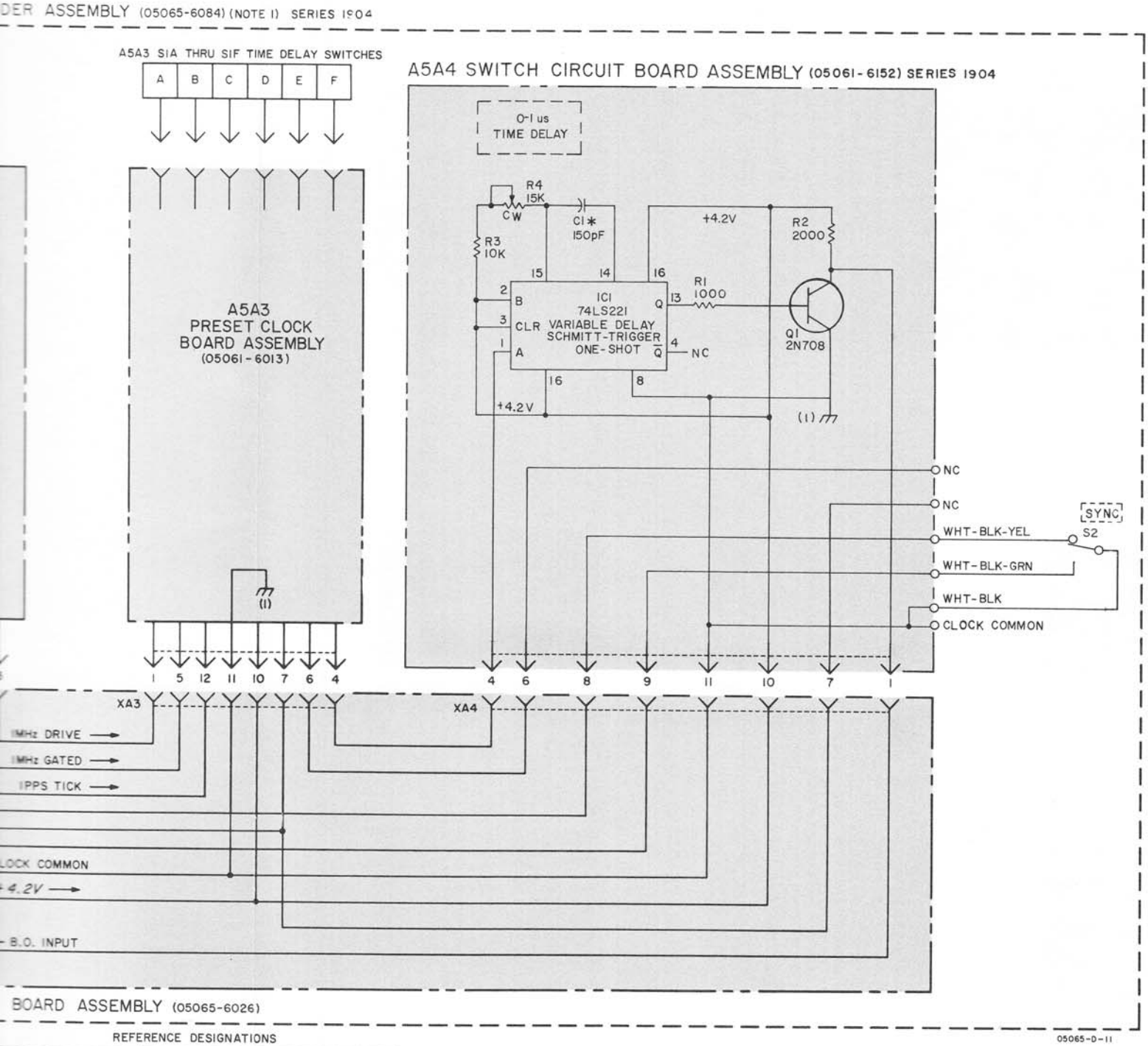
NO PREFIX	A5	A5A1	A5A3	A5A4
J5	S1-3	J1-4	S1	C1,2 IC1 Q1 R1-3

WITHIN THIS
ED. ADD
REVIATION
I.

TED:

ADS;

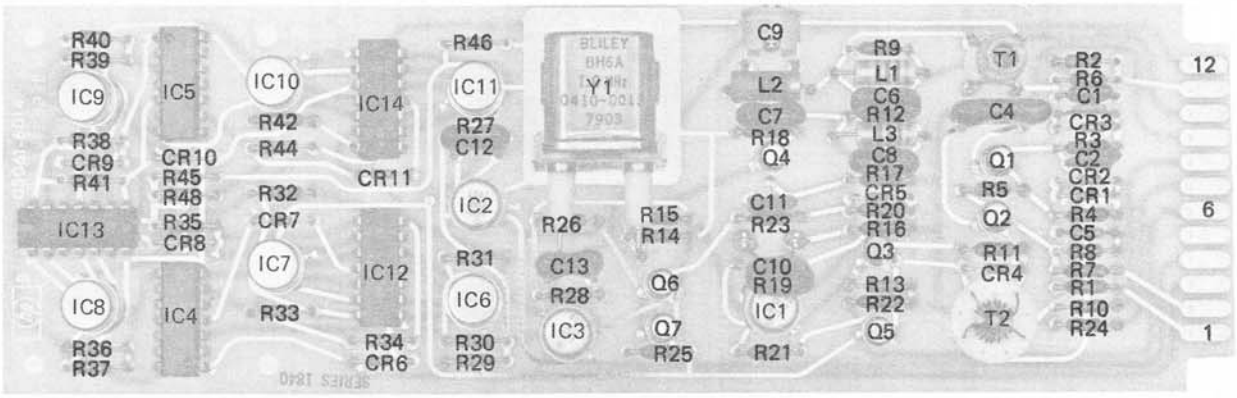
ECTED
ES SHOWN.

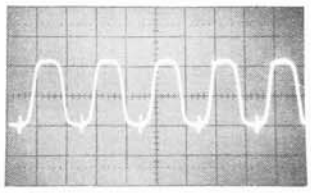


REFERENCE DESIGNATIONS

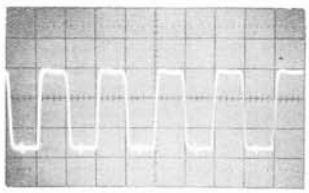
NO. EFIX	A5	A5A1	A5A3	A5A4
	S1-3	J1-4	S1	C1,2 IC1 Q1 R1-3

Figure 8-13. A5 Digital Divider Assembly (Option 001)
(Sheet 1 of 3)

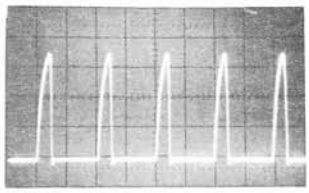




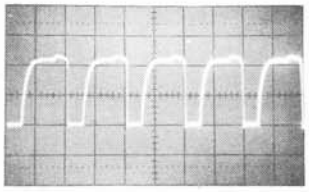
❶ (GRD DC)* .5 V/cm
.5 μs/cm



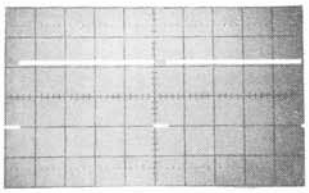
❷ (GRD Y1 CASE)
.5 V/cm, .5 μs/cm



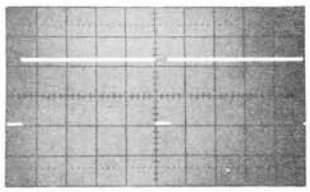
❸ 1 V/cm, .5 ms/cm



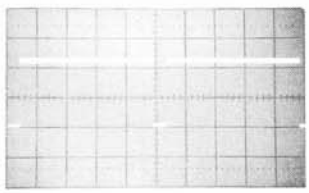
❹ 2 V/cm, .5 μs/cm



❺ 2 V/cm, .2 ms/cm



❻ (GRD Y1 CASE)
2 V/cm, 2 ms/cm



❼ (GRD Y1 CASE)
2 V/cm, .2 s/cm

*Oscilloscope:

DC coupled ground as noted.

5065A: Normal operation unless noted.

Oscilloscpe: DC coupled.

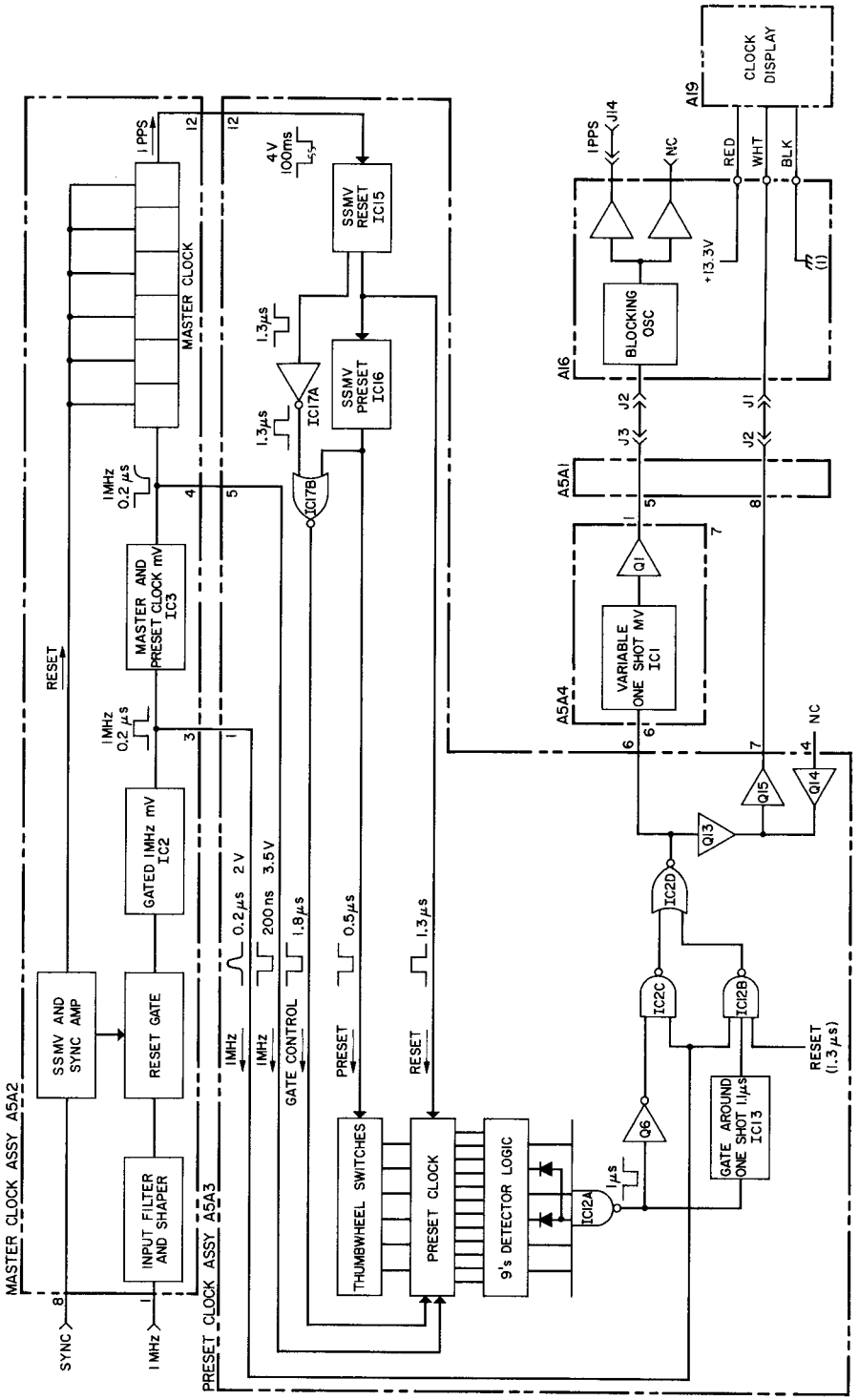


Figure 8-14
A5A2 MASTER CLOCK BOARD (OPTION 001)
(Sheet 2 of 3)

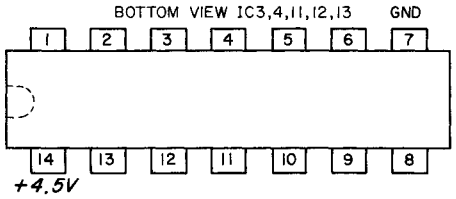
(See Page 8-35)

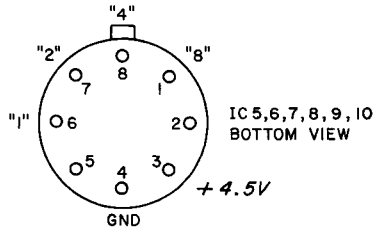
NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN.

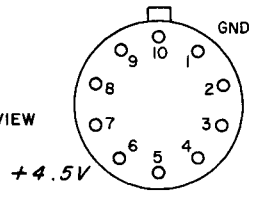
REFERENCE DESIGNATIONS

A5	A5A2
S2	C 1-13 CR 1-11 IC 1-14 L 1-3 Q 1-7 R 1-46 T 1,2 Y 1





IC 5,6,7,8,9,10
BOTTOM VIEW



IC1,2
BOTTOM VIEW

05065-D-12